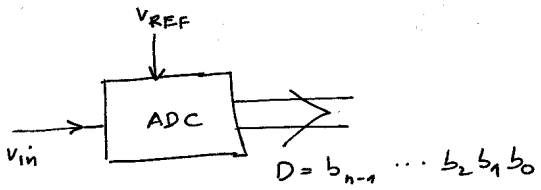
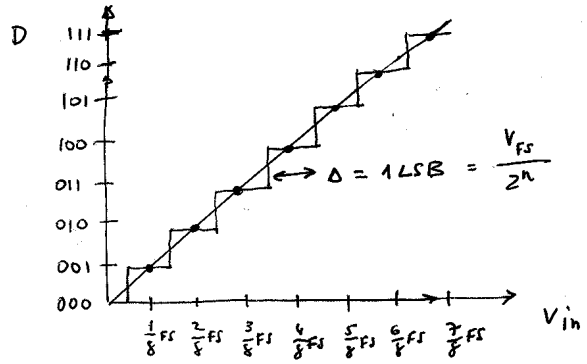
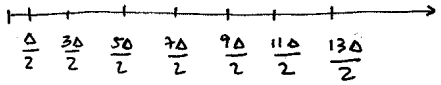
AULA 5 (INTERFACES) – CONVERSÃO ANALÓGICA-DIGITAL (ADCs)

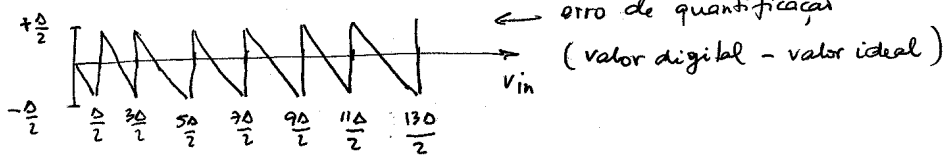


$$D = \left[2^n \frac{V_{in}}{V_{REF}} \right]$$

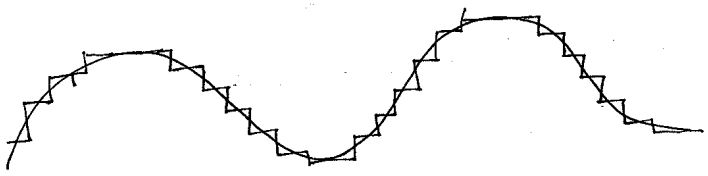
onde D é a parte inteira de $[\cdot]$ e $V_{REF} = V_{FS}$ é o valor máximo da tensão de entrada.







Sinal de entrada: <u>onda sinusoidal</u>



potência do erro de quantificação

$$\overline{\varepsilon_q^2} = \frac{1}{\Delta}\int_{-\Delta/2}^{+\Delta/2} \varepsilon_q^2 \, d\varepsilon_q$$

$$= \frac{1}{\Delta}\int_{-\Delta/2}^{+\Delta/2} x^2 \, dx = \frac{\Delta^2}{12}$$

potência de um sinal sinusoidal de amplitude $\frac{V_{REF}}{2}$

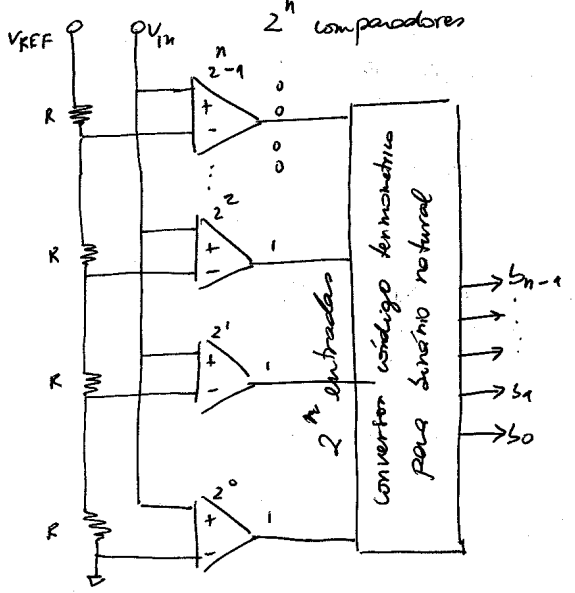
$$\overline{V_{in}^2} = \frac{1}{2}\left(\frac{V_{REF}}{2}\right)^2 = \frac{V_{REF}^2}{8} = \frac{2^{2n}\Delta^2}{8}$$

$$SNR = \frac{\overline{V_{in}^2}}{\overline{\varepsilon_q^2}} = \frac{2^{2n}\Delta^2/8}{\Delta^2/12} = \frac{3}{2}2^{2n}$$

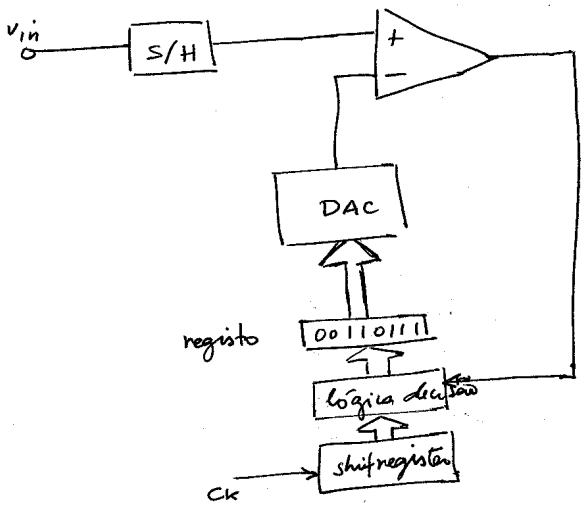
$$\boxed{SNR_{dB} = 6.02\,n + 1.76\ dB}$$

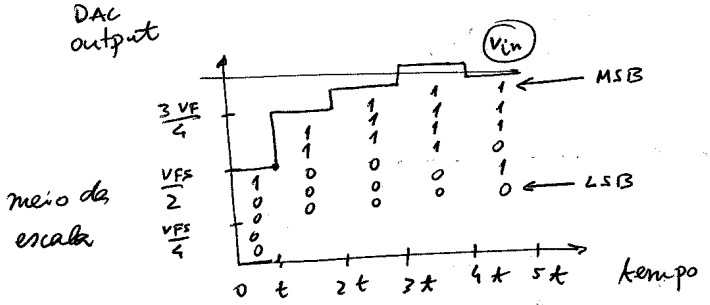
Arquitecturas para ADCs

Conversor FLASH (paralelo)



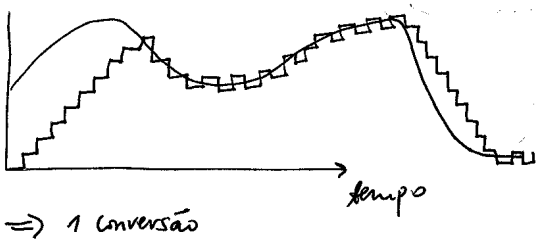
Conversor aproximações sucessivas

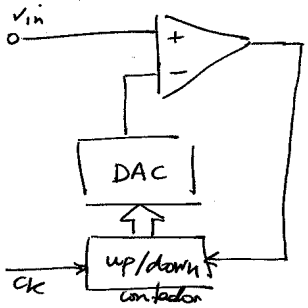




conversor de n bits ⇒ 1 conversão em n ciclos de relógio

Conversor tipo delta (tracking)





n bits ⇒ 1 conversão
2^n ciclos de relógio

Interfacing aula 5

Máxima variação do sinal de entrada (slew rate máximo)

$$\frac{dv_{in}}{dt} < \frac{\Delta}{t_{ck}}$$

Assumindo $v_{in} = \frac{V_{REF}}{2} \sin \omega t$

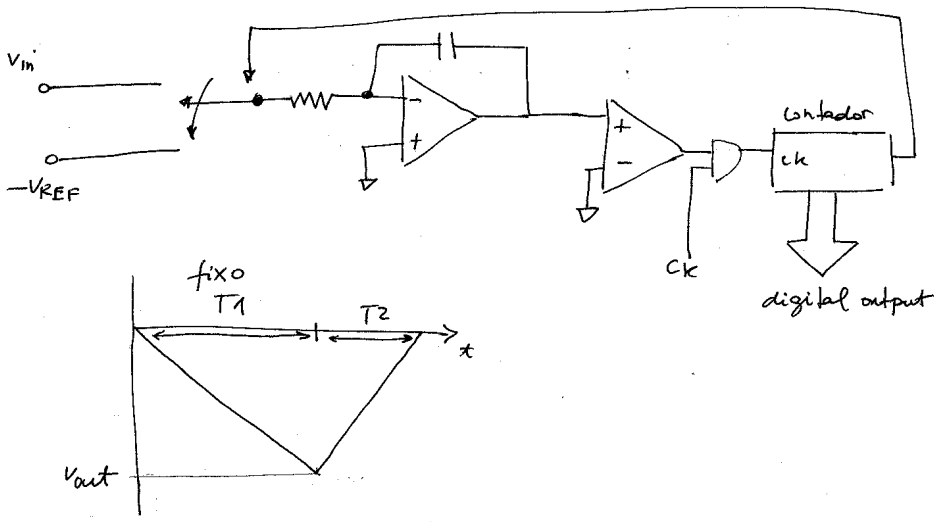
$$\max\left(\frac{dv_{in}}{dt}\right) = \max\left(\omega \frac{V_{REF}}{2} \cos \omega t\right) = \omega \frac{V_{REF}}{2}$$

$$\omega \frac{V_{REF}}{2} < \frac{\Delta}{t_{ck}}$$

$$2\pi f \frac{V_{REF}}{2} < \frac{\frac{V_{REF}}{2^n}}{t_{ck}}$$

$$\boxed{f < \frac{1}{\pi 2^n t_{ck}}}$$

Conversor integrador de dupla - rampa



1 – Condensador C é descarregado

2 – Condensador C carrega com a tensão V_{in} durante um tempo

T_1 FIXO $\quad T_1 = 2^n t_{ck}$

3 – condensador C descarrega até zero com a tensão $-V_{REF}$

durante o tempo T_2

$$Q = CV \qquad v_{out} = -\frac{Q}{C}$$

$$\frac{dv_{out}}{dt} = -\frac{1}{C}\frac{dQ}{dt}$$

$$\text{mas } \frac{dQ}{dt} = i(t) = \frac{v_{in}}{R}$$

$$\text{logo } \frac{dv_{out}}{dt} = -\frac{1}{RC} v_{in}(t)$$

$$v_{out} = -\frac{1}{RC}\int_0^{T_1} v_{in}(t)\,dt$$

$$= -\frac{1}{RC} T_1 \frac{1}{T_1}\int_0^{T_1} v_{in}(t)\,dt$$

$$V_{out} = -\frac{1}{RC} T_1 \bar{v}_{in}$$

Durante o tempo T_2

$$V_{out} = -\frac{1}{RC} T_2 V_{REF}$$

$$\text{logo } T_2 = \frac{\bar{V}_{in}}{V_{REF}} T_1$$

$$m\,t_{ck} = \frac{\bar{V}_{in}}{V_{REF}} 2^n t_{ck}$$

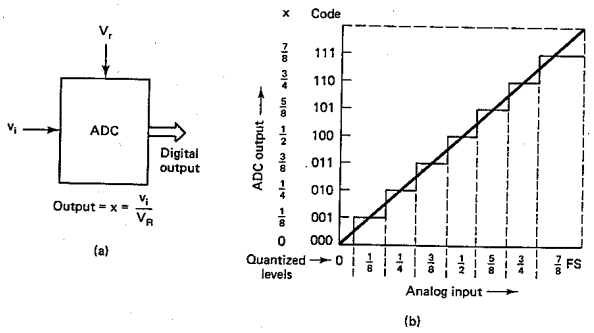


Figure 5.1 Analog-to-digital converter. (a) Basic relationship. (b) Ideal characteristics of a 3-bit ADC.

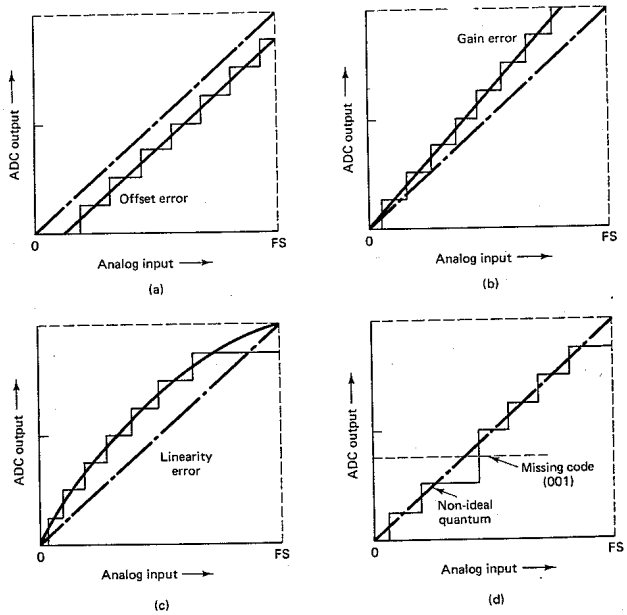


Figure 5.2 Converter errors. (a) Offset error. (b) Gain error. (c) Integral linearity error. (d) Differential linearity error.

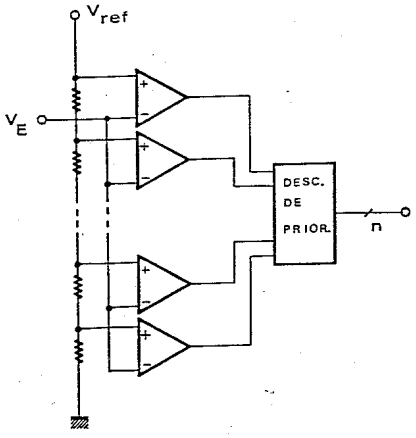


Fig.3.3 - ADC do tipo "flash" [2]

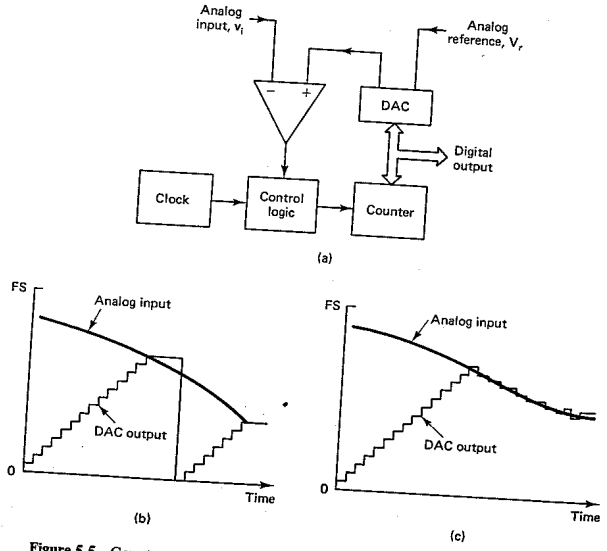
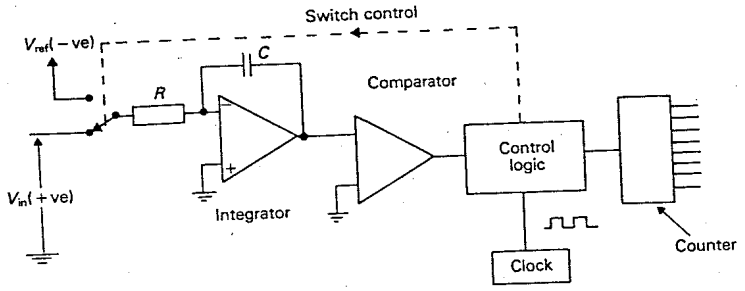
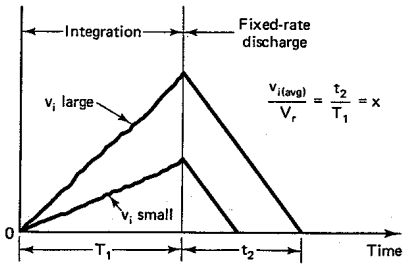


Figure 5.5 Counter or tracking-type ADC and circuit waveforms. (a) Simplified block diagram. (b) Waveforms for counter type. (c) Waveforms for tracking type.





(b)

Figure 5.7 Dual-slope ADC. (a) Block diagram. (b) Circuit waveforms.

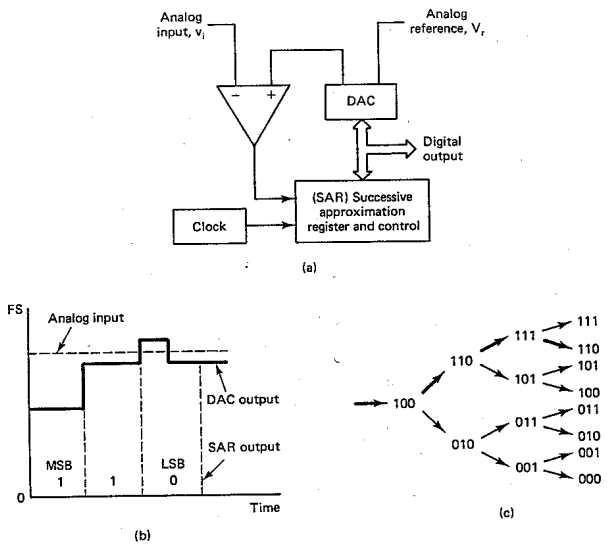


Figure 5.6 Successive-approximation ADC converter. (a) Block diagram. (b) Circuit waveforms. (c) Logic flow diagram.