CHAPTER O

Revision of Electronics 1

A: Leis de Kirchhoff

$$\sum I = 0$$

Curgas não desaperecem

$$\sum V = 0$$

voltar ao início: mesma tenção

B: ->>diodo

aberto : AV ~ 0.7 , I > 100 yA

fechado : I ~ 10-14 A (~ 0)

(indelion) C: transistor

current amplifier is

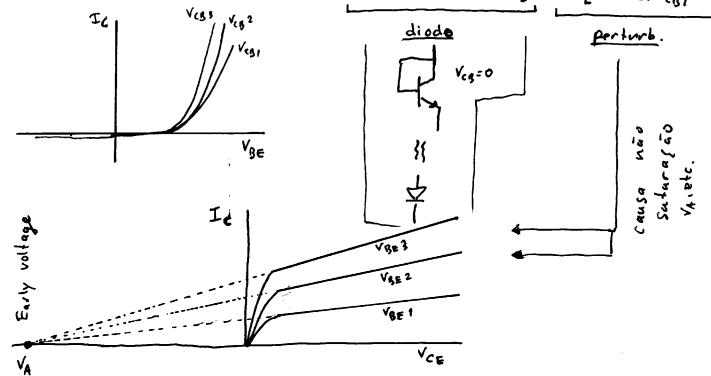
$$\begin{array}{cccc}
I_{E} &= (\beta+i) I_{B} \\
I_{C} &= \beta I_{B}
\end{array}$$

$$\begin{array}{cccc}
(Kirchhoff & I_{C} + I_{g} = I_{E}) \\
I_{C} &= \alpha I_{E}
\end{array}$$

$$\alpha = \frac{\beta}{\beta+i} \approx 1$$

typical : B=100, a= 0.99

D: Ebers - Moll: $I_c = I_o \left[\exp(\frac{2}{k_T} V_{cg}) - i \right] + I_s \left[\exp(\frac{2}{k_T} V_{cg}) - i \right]$



$$I_{E} = I_{O} \left[\exp\left(\frac{2}{\kappa_{T}}V_{BE}\right) - 1 \right]$$

$$I_{O} \sim 10^{-14} A \quad \text{reverse - bias - leakage current}$$

$$\left(V_{BE} = -\infty, I_{E} = -I_{O}\right)$$

$$I_{E} \sim I_{O} \exp\left(\frac{2}{\kappa_{T}}V_{BE}\right) = I_{O} \exp\left(\frac{V_{BE}}{V_{T}}\right) \quad V_{T} = \frac{\kappa_{T}}{2}$$

$$\text{correcte tipica: } T\text{ in A}, \quad T = 300\text{ k} \left(V_{T} = 26\text{ mV}\right)$$

$$V_{BE} = V_{T} \ln\left(\frac{I_{E}}{I_{O}}\right) : \quad 0.60 \text{ V} \iff 100 \text{ yA}$$

$$0.66 \text{ V} \iff 1 \text{ mA}$$

$$0.72 \text{ V} \iff 100 \text{ mA}$$

$$r_i = \frac{1}{\partial I_i}$$
 example ∂I_i

example:
$$V_i = V_{gE}$$

$$I_i = I_8 = \frac{1}{(\beta / i)} I_E$$

$$\frac{\partial T_{i}}{\partial V_{i}} = \frac{1}{(\beta+i)} \frac{\partial T_{E}}{\partial V_{gE}} = \frac{\underline{T_{o}}}{(\beta+i)V_{T}} exp\left(\frac{V_{gE}}{\widehat{V_{T}}}\right) = \frac{\underline{T_{E}}}{(\beta+i)V_{T}}$$

$$\Gamma_i = (\beta+i) \frac{V_r}{I_E} = [\beta+i) \Gamma_e = \Gamma_{\pi}$$

$$R_i \equiv \frac{1}{V_i}$$

example :
$$R_i = \frac{1}{\rho_{ij} V_{RE}}$$

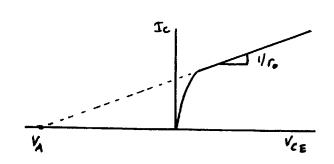
note:
$$g_m = \frac{\partial I_{out}}{\partial V_i} = \frac{B \partial I_i}{\partial V_i} = \frac{B}{B+1} \frac{1}{f_e}$$

re is a <u>parameter</u> that describes the <u>dynamic</u>
response to a signal input (δV_i) . It is not a real
resistance! $V_i = \delta V_i$ $V_i = \delta V_i$ $V_i = \delta V_i$ $V_i = \delta V_i$

$$\Gamma_0 \equiv \frac{1}{2} \frac{\partial \Gamma_0}{\partial V_0}$$

exemple : transister

$$I_0 = I_C$$
 $V_0 = V_C = V_{CE}$

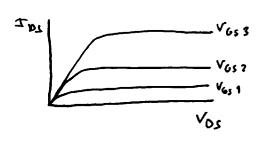


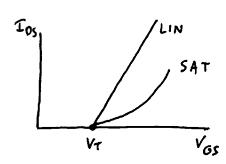
$$\frac{\partial I_o}{\partial V_o} = \frac{\partial I_c}{\partial V_{CE}} = \frac{I_c}{V_{CE} + V_A}$$

$$\Gamma_0 \sim \frac{V_A}{T_C} ex = \frac{200 \text{ V}}{1\text{mA}} = 200 \text{ KSZ}$$

LIN:
$$I_{ds} = \left(V_{ox} \right) \frac{W}{L} \left(V_{Gs} - V_{T} \right) V_{OS}$$

SAT:
$$T_{ds} = \frac{1}{2} \left(o_X y \frac{W}{L} \left(V_{GS} - V_T \right)^2 \right)$$





$$f_0 = \frac{1}{\partial I_{ps}} = \infty$$

$$\Gamma_i = \frac{1}{\partial T_G} = \infty \left(T_{GS} = 0 \right)$$

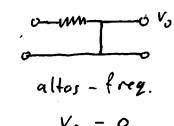
"em altar frequências um C é um curto-circuito" em baixas frequências um C é um circuito-aberto "

(LPF) (low-pass filter)

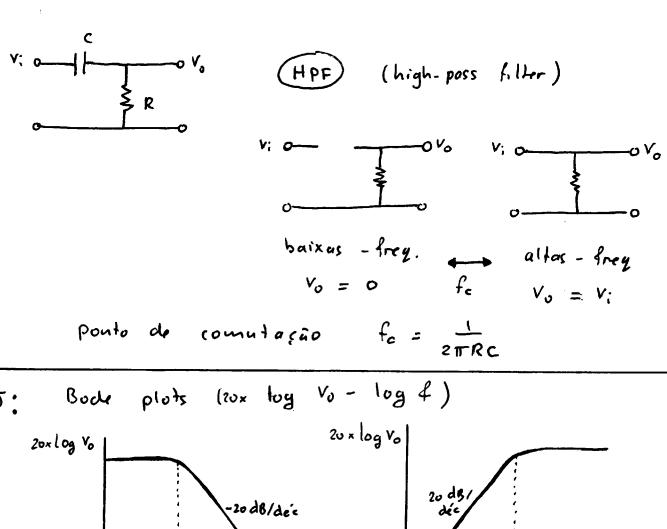
V: 0-mm o Vo

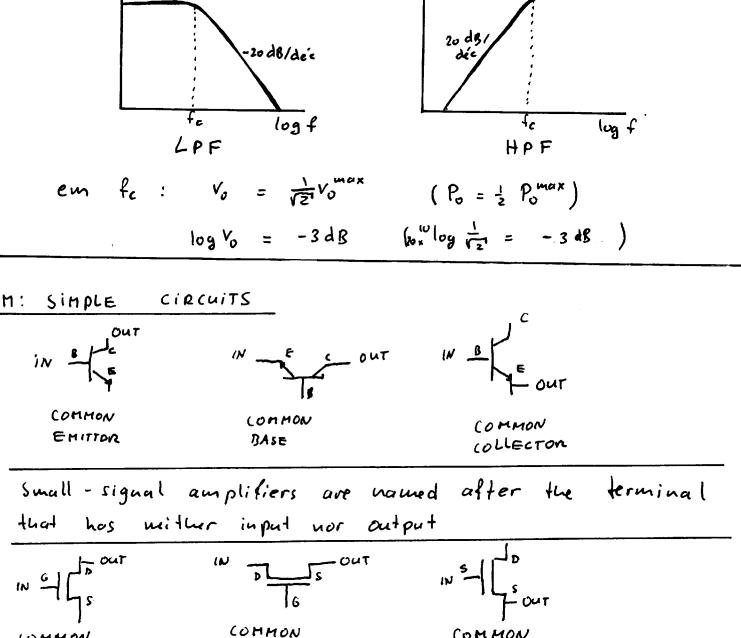
baixus - freq.

$$V_0 = V_1$$
 $V_0 = V_1$
 $V_0 = V_1$



ponto de comutação: fe = TRPC





GATE

LUMMON

SOURCE

COMMON

DRAIN

(-3d0)

$$T(4) \equiv V_o(f)/V_i(4)$$

$$\frac{LPF}{1}$$

$$\frac{1}{1+s/\omega_{o}}$$

$$\frac{s}{s + \omega_o}$$

HPF

$$T(\omega)$$
 $\frac{1}{1+j\omega/\omega_o}$

$$|T(\omega)| = \frac{1}{\sqrt{1 + (\omega/\omega_0)^2}}$$

$$\sqrt{1 + (\omega_0/\omega)^2}$$

0

$$\omega = \infty$$

 $\omega = cs$ $\omega = \omega_0 \quad |T| = \frac{1}{\sqrt{2}}, \quad \phi = -45^\circ$

|T| = 1/2, Ø = +45° ~ W (20 ds/dec)

w << wo

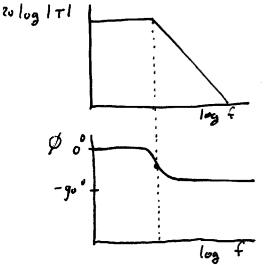
~ /w (-20 dB/dec)

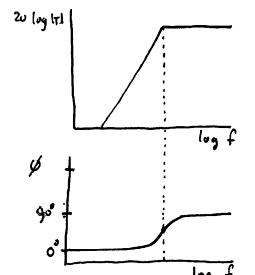
 $\omega_o =$

1 RC

RC

Bode Plots

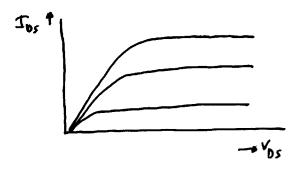


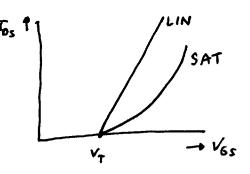


H: Field - Effect Transistor

LIN:
$$I_{ds} = (o_{x} y \frac{w}{L} (V_{Gs} - V_{T}) V_{Os} = \lambda (V_{Gs} - V_{T}) V_{Os}$$

 SAT : $I_{ds} = \frac{1}{2} (o_{x} y \frac{w}{L} (V_{Gs} - V_{T})^{2} = \frac{1}{2} \lambda (V_{Gs} - V_{T})^{2}$





$$\begin{aligned}
\Gamma_0 &= \left| \frac{\partial I_{0s}}{\partial V_{0s}} \right| = co & \Gamma_i &= \left| \frac{\partial I_{0s}}{\partial V_{0s}} \right| = co & (I_{0s} = 0) \\
& \text{(no leakage (urrent or polarization current!)} \\
9m &= \left| \frac{\partial I_{0s}}{\partial V_{0s}} \right| = \lambda V_{0s} & (LIN)
\end{aligned}$$

$$= \lambda V_{G}, \qquad (SAT)$$

L: components analyzed

- A resistance is a linear element that translates current to voltage

A resistance defines a current

$$V \rightarrow I$$

c = Q/V

A capacitor is a charge storage

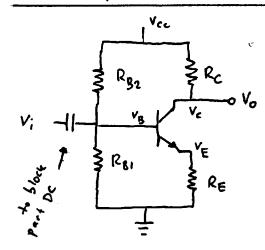
"haw much charge stored per volt"

V

Q

is "integrator"

 $\int Idt \rightarrow V$



$$\beta = 100$$
 $R_{B1} = R_{B2} = 10 \text{ k.s.}$
 $R_{E} = 3.3 \text{ k.s.}$
 $R_{C2} = 3.3 \text{ k.s.}$
 $R_{C3} = 3.3 \text{ k.s.}$

POLARIZATION / BIAS

$$v_{g}$$
?

Assumption Fig at transistor >> 10 K why? ri = ry + RE? No!

Femewher:
$$\Gamma_i = \frac{1}{\partial V_R}$$

$$\frac{\partial I_{g}}{\partial V_{g}} = \frac{\int_{\beta+1}^{1} \partial I_{E}}{\partial (V_{E} + 0.7 V)} = \frac{1}{\beta+1} \frac{\partial I_{E}}{\partial V_{E}} = \frac{1}{(\beta+1)} R_{E}$$

$$\frac{1}{\beta+1} \frac{\partial I_{E}}{\partial V_{E}} = \frac{1}{(\beta+1)} R_{E}$$

$$I_{mplies}$$

$$I_{m=0}$$

$$I_{m=0}$$

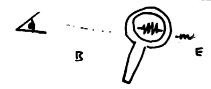
total (including
$$r_{\pi}$$
): $r_{i} = r_{\pi} + (\beta+1) R_{\Xi}$

Order order

(1652 (00 kg.

 $\Gamma_{i} = \Gamma_{TT} + (\beta + i) R_{E}$

O transistor funcione como uma lente. Vista da base. as resistências (e outros componentes) apere cem ampliadas.

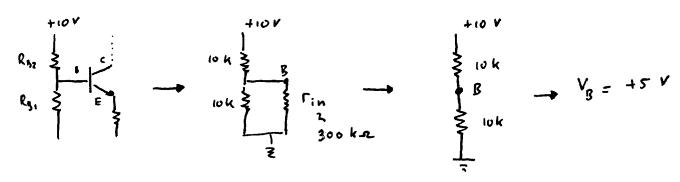


(β+1)RE ←

na base aperecem reduzidos



Vista do emisor, os componentes



$$V_{R} = \frac{R_{R_1}}{R_{R_1} + R_{R_2}} - V_{Ce} = \frac{10 \text{ kg}}{10 \text{ kg} + 10 \text{ kg}} \cdot 10 \text{ V} = 5 \text{ V}$$

$$V_E = V_B - 0.7 V$$
 (in case transistor open, check at end!)
$$= 4.3 V$$

$$I_{B} = I_{E}/(\beta+1) = 12.9 \text{ yA}$$

$$I_{C} = \alpha I_{E} = 1.29 \text{ mA}$$

$$V_{cc} = \frac{10V}{R_c}$$
 $V_o = V_{cc} - R_c \cdot I_c = 10 - 3.3 \text{ kg} \times 1.29 \text{ mA} = 5.74 \text{ V}$
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 $V_o = V_o = V_o = V_o = V_o = V_o = 10 - 3.3 \text{ kg} \times 1.29 \text{ mA} = 5.74 \text{ V}$

$$5.74V$$
 C
 n
 $-5.74V$
 E
 n
 $-5V$
 $-4.3V$

A properly working transistor has the C-B biased reverse and the B-E junction in forward. Forward bias: n = negative, p = positive. Thus, the above transistor is working correct.

$$r_e = \frac{V_T}{T_E} = \frac{26 \text{ mV}}{1.30 \text{ mA}} = \frac{20 \text{ SZ}}{1.30 \text{ mA}}$$

Total dynamic input resistance of amplifier:

For AC signals: any DC power supply point is equal to 1 (and current source = one souther a opin)

(because v (= &v) = 0!

Fin= Rg, // Rg2 // Fin = 10 Ks // 10 Ks // 335 Ks ~ 5 ks

AC signal amplification:

 $\Gamma_i = \Gamma_{\pi} + (\beta + i) R \in$

$$\Gamma_{i} \equiv \frac{1}{2} \frac{\partial I_{g}}{\partial V_{g}} \implies \partial I_{g} = \frac{\partial V_{g}}{\Gamma_{i}} = \frac{\partial V_{g}}{\Gamma_{\pi} + (\beta + i)R_{E}}$$

$$I_c = \beta I_g \implies \partial I_c = \beta \partial I_g = \frac{\beta \partial V_g}{\Gamma_{\pi} + (\beta + i) R_E}$$

$$V_o = V_{cc} - R_c I_c \implies$$

 $\partial V_0 = -R_c \partial T_c = -\frac{\beta R_c}{}$ ∂V_B

(T + (B+1) RE minusulas maingenlas

$$A = \frac{V_o}{V_B} = \frac{\partial V_o}{\partial V_B} = -\frac{R_c}{r_e + R_E} \qquad (r_{\pi} = (\beta + 1)r_e, \beta \approx (\beta + 1))$$

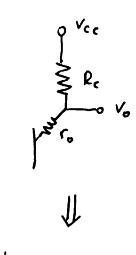
The gain of a common-emittor

amplifier is all resistance at collector

Re divided his M divided by all resistance at emittor with minus sign

$$A = -\frac{3300}{20 + 3300} \sim -1$$

output resistance of amplifier



(vith E connected to ground!!)

ro & 200 k. (p.3)

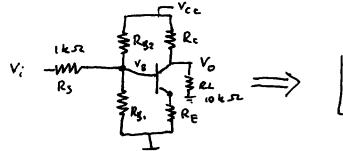
(ro >> Rc)

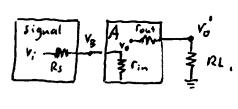
Fout of transistor in Com. Em. is Much larger than ro (something like & F. F. of ch. 1)

fout N Rc = 3.3 km

Combining amplifier stages

imagine signal source has I ks output resistance and what will be the total gain of circuit?





 $R_{s} = 1 \text{ k.s.}$, $r_{in} = 5 \text{ k.s.}$ (p.7), $R_{L} = 10 \text{ k.s.}$ A = -1 (p.7) , $r_{out} = 3.3 \text{ k.s.}$ (p.8)

$$A_{+o+} = \frac{v_o'}{v_i} = \frac{v_o'}{v_o} \cdot \frac{v_o}{v_g} \cdot \frac{v_g}{v_i}$$

$$\frac{V_0'}{V_0} = \frac{RL}{R_L + r_{out}}, \quad \frac{V_0}{V_B} = A, \quad \frac{V_0}{V_i} = \frac{r_{in}}{r_{in} + R_S}$$

$$= 0.429 \qquad = -1 \qquad = 0.832$$

Atot = 0.429 x -1 x 0.033 = -0.357

DC power consumption of amplifier

Rose Nok Re 3.3K

 $\rho = I^2 R$ or V^2 / R or VI

RBI: V = 5V, R = 10 K => P = 2.5 mW

RB2: V = SV , R = 10 k = P = 2.5 mW

RE: V= 4.3 V R= 7.3 K => P= 5.6 mW

Rc: V = 4.3 V, R=3.34 => P=5.6 mW

* trans : V = 0.7 V, I = 1.29 mA => P = 0.90 mV

total P= 17.1 mm

Note: there is power loss at every part where we have a voltage drop and a current simultaneously. You can also say: where there is a current and a resistance. The heat generated in the transistor is not much in this case, but other amplifiers will lose a lot of power in the transistors and have to be cooled.

and have to be cooks.

* note that we cannot use re or to here because they ove for Signals (AC) only.

Alternative calculation: The tov power supply supplies a total current of 1.29 wA through Re plus 0.5 mA ($\frac{+10V}{(0K+10K)}$) through the base resistors. Total: 1.79 mA. P=V.T=17.9 mW

N: Small-signal models of transistors and amplifiers.

Although electronic circuits can be analyzed without the help of small-signal models, in some cases those small-signal model can help to understand things. Examples of BJT models

Hybrid - IT model with Hybrid - IT model with current controlled voltage - controlled current source current source (gm Vbe 11 T model with voltage -T model with current controlled current source controlled current

BASIC BJT AmpliFIERS

0:

COMMON - EMITTER AMPLIFIER (CEA)

V: $\frac{V_0}{V_1} = \frac{R_c}{V_e + R_E}$ Vi = $(\beta+1)(\Gamma_e + R_E)$ Fout = R_c

Common - BASE AMPLIFIER (CBA)

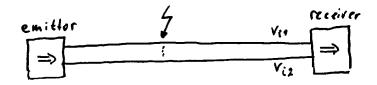
gain
$$\frac{v_0}{v_i} = \pm \frac{R_c}{r_e}$$

common - collector Amplifier (CCA)

gain
$$\frac{v_0}{v_i} = \frac{R_E}{(r_e + R_E)} \approx 1$$

A differential amplifier has two inputs and two outputs. The difference voltage at the output is proportional to the difference voltage at the input

The advantage is obvious. For transmission lines, the noise is reduced



whatever noise is introduced in the line, this noise is normally equal in both line. (The noise is "correlated"). Therefore, the difference is zero. $V_{i2}-V_{i4}=0$. All noise will be rejected. Most communication lines work like this (twisted-pair network cubes, etc.). The differential amplifier is therefore are of the most important electrical circuits.

An ideal diferencial amplifier thus reject all signals that appear on both terminals. We can define this in the common-mode rejection ratio (CMRR). This is the ratio of the gain at common mode

 $A_{cm} = \frac{v_o}{v_i} \qquad \text{with} \quad v_o = v_{o_1} = v_{o_2} \quad \text{and} \quad v_i = v_{i_1} = v_{i_2}$ and the differencial gain

$$A_{dm} = \frac{V_{02} - V_{01}}{V_{i2} - V_{i1}}$$

Then

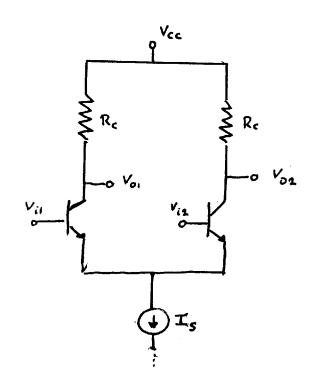
$$CHRR = \left| \frac{A_{dm}}{A_{cm}} \right|$$

This should be as high as possible. The CMRR is an important parameter to qualify a differencial amplifier.

Other aspects are cost (number of components), power consumption and possibility to fabricate in integrated circuits.

One of the most popular is the differential pair (par differencial).

Par Diferencial (Bogart: ch 12)



A basic differential pair

consists of two (npn) transistors,
a current source (Is) and

current-to-voltage converters Rc

We will calculate the gains (Acm
and Adm) and CMRR for different

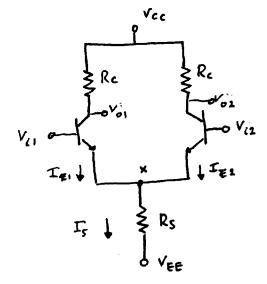
versions of this basic model

1: Is defined by a simple resistance

2: Is a current source made with a transistor

3: current-to-voltage converters made of prop transisters

Model 1



Re = 3.3 K.R. Rs = 10 k.R. V(c = +10 V, VEE = -10 V Esimple DP current source is a resistance. Why can we call it a current source? Because the DC voltage at x (the emittors of both transistors) is $v = 0.7 \ v$ (assuming small signals at v_{ij} and v_{ij} and no DC components)

Thus $T_s = (-0.7 - V_{EE})/R_s$

Polarization: Vi = Viz = 0 V

Vx = -0.7 V. Is = (-0.7 + 10) / 10 kp = 0.93 mA.

Because of symmetry: I = I = 1/2 Is = 0.465 mA.

 $\beta = 100 \implies 0.7$ $I_{c1} = I_{c2} = 0.465 \text{ mA} \implies V_{01} = V_{02} = 10 \text{ V} - 0.465 \text{ mA} \cdot 334$

$$f_e = V_T/I_{E1} = 56 - \Omega$$
 = 8.47 V

Did we design this DP well? No!

0 V = 8.5 V

The output can swing up to 10 V and down to v OV. This gives us a maximum

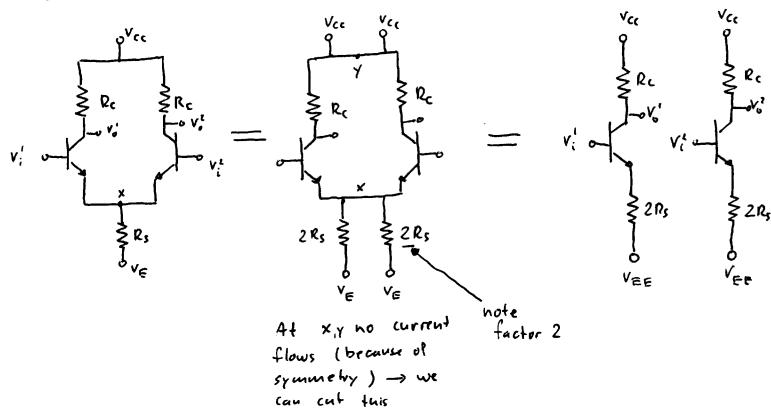
0 × ////////

output signal of ~ 1.5 V amplitude. Had we designed the DP to have a bias at 5 V, the maximum output signal would have been 5 V. Options: increase Rc Ito 10.8 km) or decrease Rs (to 3.1 km)

But ... let's continue with this poor DP

Common Mode Gain (Acm).

since at all points on the left the voltages and currents are exactly the same as their counterpoints on the right, we can use a trick of symmetry:



To calculate $A_{cm} = \frac{V_0}{V_1^i}$ is no problem. This is a normal common emitter amplifier:

Alternative way of analyzing (for those who don't like to use tricks and laws of physics) similar to p.5 of ch.0

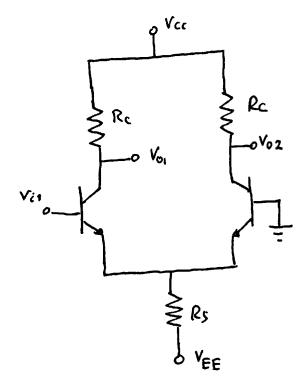
$$A_{cm} = \frac{\partial V_{0i}}{\partial V_{ii}} \Big|_{V_{i1} = V_{i2}}$$

$$\frac{\partial I_{g_1}}{\partial V_{g_1}} = \frac{1}{\beta^{+1}} \frac{\partial I_{E1}}{\partial (V_{E1} + 0.7V)} = \frac{1}{\beta^{+1}} \frac{1}{2} \frac{\partial I_{S}}{\partial V_{X}} = \frac{1}{2(\beta^{+1})} \frac{1}{R_{S}}$$

$$\frac{\partial V_0}{\partial V_0} = \frac{\partial V_{01}}{\partial V_0} \cdot \frac{\partial I_{01}}{\partial V_0} = -R_c \cdot \beta \cdot \frac{1}{(\beta+1)} \cdot \frac{1}{\Gamma_0 + 2R_c} = -\frac{R_c}{\Gamma_0 + 2R_c} \quad q.e.$$

$$Adm = \frac{V_{02} - V_{01}}{V_{i2} - V_{i4}}$$
.

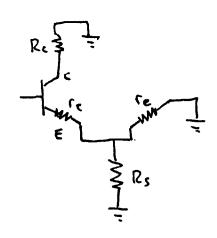
For our analysis we will connect the second input to ground $(v_{i2}=0)$



Adm =
$$\frac{V_{01}}{V_{i1}} - \frac{V_{02}}{V_{i1}}$$

Single - ended
common - mo de
gain

To calculate the gain $\frac{V_{01}}{V_i}$ is easy: All resistance at collector divided by all resistance at emitter.

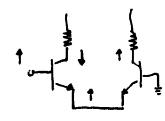


$$\frac{V_{01}}{V_{i1}} = -\frac{R_c}{\Gamma_e + \Gamma_e // R_S} \sim -\frac{R_c}{2\Gamma_e}$$

This is the single-ended Dn gain Adm

The other output has the same gain,
but with positive sign

$$\frac{V_{oz}}{V_{ia}} = + \frac{Rc}{2re}$$
 why?



 V_{i1} increases \rightarrow V_{BE1} increases \rightarrow I_{C1} increases \rightarrow V_{O1} decreases \rightarrow negative sign

Via increases -> VEA increases (albeita little less) ->

VBEZ decreases -> IBZ dereases -> Icz decreases
-> Voz increases.

Another way to understand this:

Because we have a <u>current source</u>, the current is constant $I_{E1} + I_{E2} = constant \Rightarrow i_{e_1} = -i_{e_2} \Rightarrow i_{e_2} = -i_{e_2} \Rightarrow i_{e_2} = -i_{e_3}$ $V_{02} = -i_{e_4}$ $V_{02} = -Ri_{e_2}, V_{01} = -Ri_{e_4}$ $V_{02} = -V_{01}$ $V_{01} V_{02}$ R_c R_c

 $\boxed{Adm} = \frac{V_{01}}{V_{i1}} - \frac{V_{02}}{V_{i1}} = -\frac{R_c}{2 \Gamma_e} - \frac{R_c}{2 \Gamma_e} = \boxed{-\frac{R_c}{\Gamma_e}} = -58.9$

CMRR = $\left| \frac{A_{dm}}{A_{cm}} \right| = \left| \frac{-R_c/r_e}{-R_c/(r_e + 2R_s)} \right| = \frac{2R_s + r_e}{r_e} = 358$

To improve the CMRR we should increase Rs in some way. The best way to do it is to replace Rs with a current source. Theoretically rout = 00 (ideal current source)

(Model 2)

 $Acm = \pm \frac{Rc}{r_e + 2r_{out}} = 0 \quad (ideal)$

$$Adm = -\frac{R_c}{r_e}$$

CMRR =
$$\frac{2r_{al}+r_{e}}{r_{e}}$$
 = ∞ (ideal)

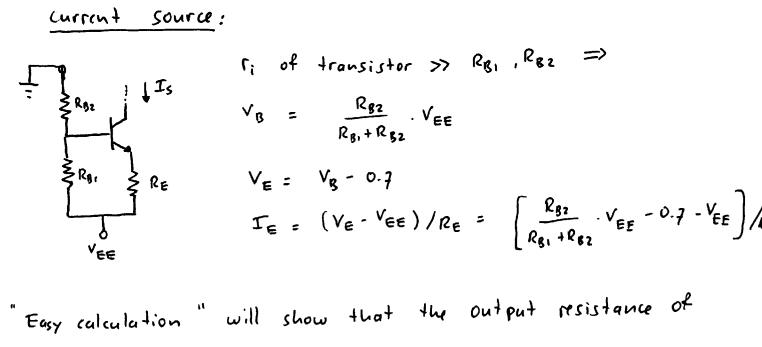
The problem now boils down to:

how to make a current source with

maximum rout. The "current source" of model 1 is rather

poor and has an rout of Rs (n ksz's)

current source:



$$V_{B} = \frac{R_{g2}}{R_{g_1} + R_{g_2}} \cdot V_{EE}$$

$$I_{\epsilon} = \left(V_{\epsilon} - V_{\epsilon \epsilon}\right) / R_{\epsilon} = \left[\frac{R_{g_2}}{R_{g_1} + R_{g_2}} \cdot V_{\epsilon \epsilon} - 0.7 - V_{\epsilon \epsilon}\right]$$

"Easy calculation" will show that the output resistance of this current source is

$$r_{out} = r_o + \left[(r_{\pi} + R_g) // R_E \right] + \frac{r_o \beta R_E}{r_{\pi} + R_g + R_E}$$

with ro equal to output resistance of transistor $\left(\frac{VA}{T_E}\right)$

$$r_{\pi} = (\beta + 1) r_{e}$$

Example: Rg1 = 10 kx, Rg2 = 10 kx, RE = 4.7 kx

$$V_{B} = -5V$$
, $V_{E} = -5.7V$, $I_{E} = 0.91 \text{ mA} \Rightarrow I_{3} = 0.91 \text{ mA}$

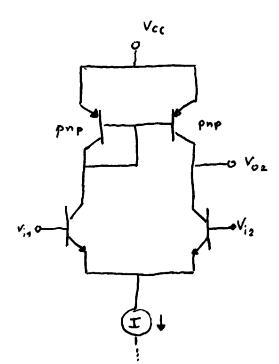
$$Acm = -2.0 \cdot 10^{-4}$$
 $Adm = -58.9$ (unchanged)

CMRR =
$$\left| \frac{-58.9}{-2.0 \cdot 10^{-4}} \right| = 2.9 \cdot 10^{5}$$
 (800 times better!)

To further increase the CMRR we can try to increase the differential gain Adm. Remember

So we should increase Rc. This can be done by replacing the collector resistances by (pnp) transistors, whose output resistance is ro (100's ks2):

Differential pair with active load



$$A_{cm} = -\frac{r_o}{r_{e+2}r_{ou}}$$

In our example re= 56 sc:

The advantage of the active load is not a higher CMRR. So why are all DP's implemented with active load?

The reason is the fact that there are no resistances in the circuit las we will see, the current source can be made by current mirrors). In integrated circuits it is very difficult to make resistances (where it is easy to make transistors).

One final observation. We used here the single-ended gain /output. Only Voz. In fact, the gain at voi is much lower. When we connect viz to ground (differential mode):

$$\frac{V_{01}}{V_{i1}} = -\frac{r_{\pi}^{r}//r_{\pi}^{r}}{2r_{e}^{n}} \approx -\frac{B}{4}$$

$$\left(\begin{array}{ccc} r_{\pi}^{p} & \text{is of pup} & r_{e}^{h} & \text{of npn tr.} \\ (r_{0}^{r} & \text{is of pup}) & \\ (r_{0}^{r} & \text{is of pup}) & \\ A_{dm} \approx -\frac{r_{0}^{r}}{2r_{e}} & \\ \end{array}\right)$$

$$A_{dm} \approx -\frac{r_{0}^{r}}{2r_{e}}$$

common mode (vi, = Viz)

$$\frac{V_{01}}{V_{01}} = -\frac{r_{\pi}^{\rho}//r_{\pi}^{\rho}}{r_{e}^{\rho}+2r_{o}^{s}}$$

$$V_{02}$$

$$V_{i1} = -\frac{r_{o}^{\rho}}{r_{e}^{\rho}+2r_{o}^{s}}$$

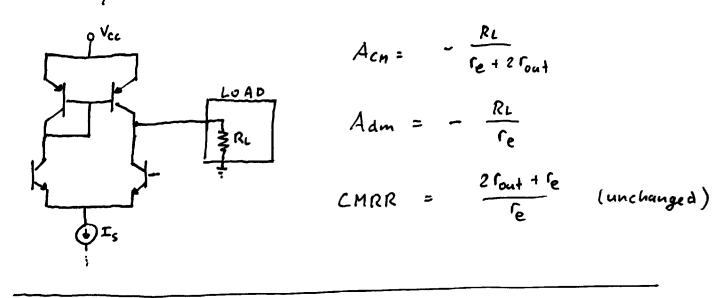
$$A_{cm} \approx \frac{r_{o}^{\rho}}{2r_{o}^{s}}$$

CMMR = $\frac{\Gamma_0^5}{\Gamma_0}$ (A factor 2 less than of p.8)

A fact that is not found back in textbooks.

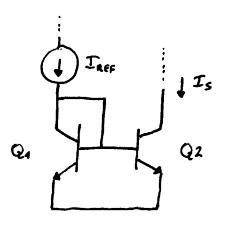
one more observation about the DP with active load:

This is a strange amplifier, because the input signal is voltage, but the output signal is rather <u>current</u>. (ideally, $r_0^p = \infty$). This amplifier only works when connected to something. In that case the gain becomes limited by the load resistance.



CURRENT SOURCES

we already used a current source (on p.7) and, as a matter of fact, the active load in the previous amplifier is also a current source, a so-called current mirror. It is called a mirror, because the current in one leg (the right in this case) is equal to the current in the other leg (left in this case). The reason why this is so is easy to see. (onsider the next circuit of a current mirror:



Is is equal to IREF! Why

Imagine IREF is from ideal current saurce. This current is 'pushed' through transistor Q1. ("at all cost"). Therefore,

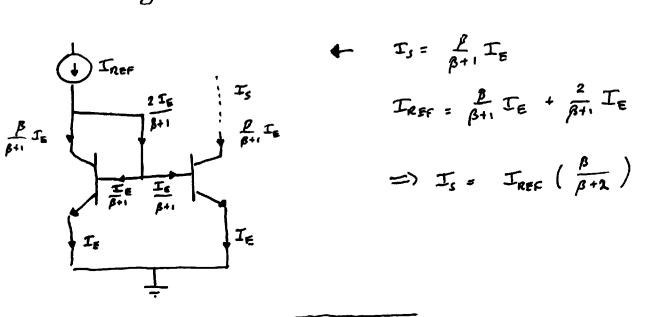
a voltage drop V_{RE1} is induced at the base-emittor junction. According to Ebers-Moll (p.2 ch.0) for a cliode $I_{E1} = I_{REF} = I_0 \exp\left[\frac{V_{RE}}{V_T}\right]$

$$\Rightarrow V_{gei} = V_{\tau} \ln \left(\frac{I_{REF}}{I_{o}} \right)$$

The voltage drop at the right transistor is equal (same base and same emittor voltages). $V_{RE2} = V_{BE4}$. Therefore, $I_{C2} = I_{C1} = I_{REF}$. (using Ebers-Moll).

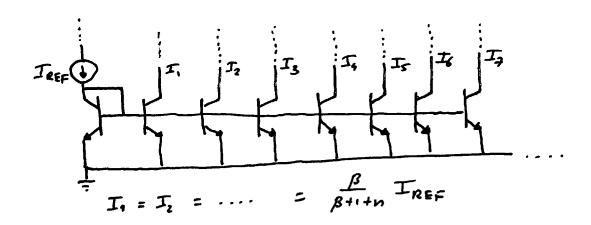
Here we have assumed an infinite B. For finite B we can see that a little bit of the current Tree is lost

for biosing the transistors.



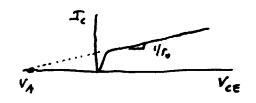
We started with a current source (TREF) and ended with

Multi - current - source



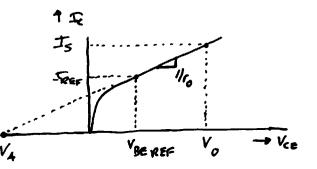
The output resistance of a current mirror is to (~ VA/I.)

Ics depends on

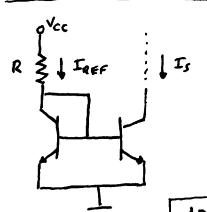


This causes another non-linearity. Since the current the collector voltage, the source current depends on the output voltage, and is not necessarily equal to IREF (VCREF = VBREF

 $\neq V_{c_1}$). $I_{s} = I_{REF} + \left(V_{o} - V_{BE,REF}\right)/r_{o} = I_{REF}\left(1 + \frac{V_{o} - V_{BE}}{V_{A}}\right)$



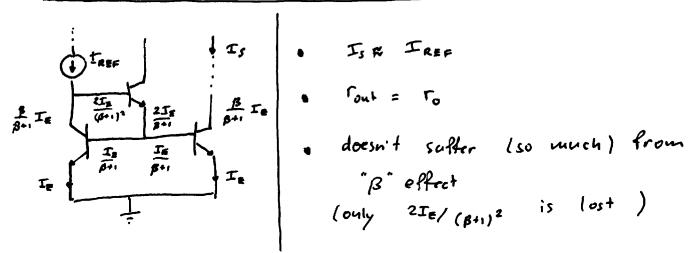
Other current sources / mirrors:



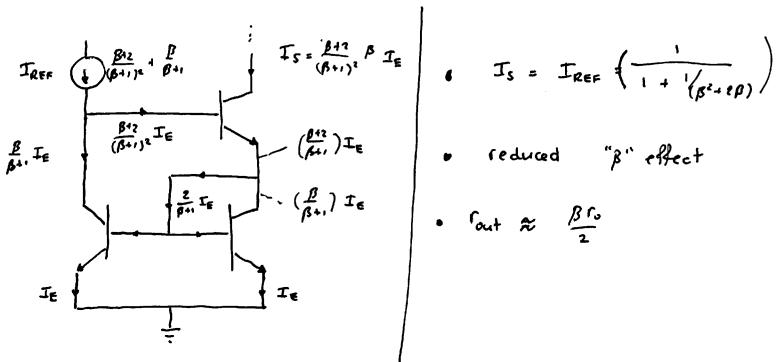
•
$$T_s = \frac{V_{cc} - 0.7}{R}$$

(suffers from "B" and "Vo" effects)

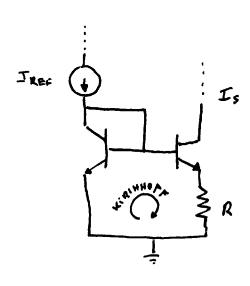
R TURNS A MIRROR INTO A SOURCE! ADDING



WILSON CURRENT MIRROR



$$I_{S} = I_{REF} \left(\frac{1}{1 + \frac{1}{(\beta^{2} + \ell \beta)}} \right)$$



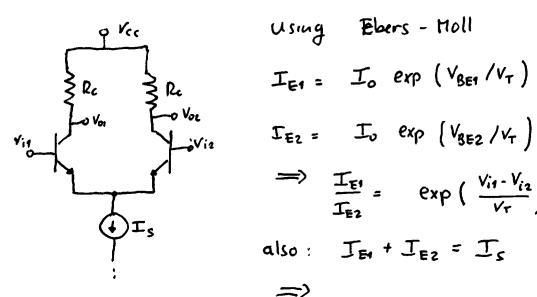
$$V_{\text{BES}} = V_T \ln \left(\frac{I_s}{I_b} \right)$$

(still possible with integr. circuits) · R very small

IREF & IS

LARGE - SIGNAL ANALYSIS OF D.P.

until now it was assumed that we worked in the linear region of the D.P. That is von Vi. Up to what point was this justified?



Using Ebers - Moll

VBE1 = Vi1 - VE VBE? = Viz -VE

$$\Longrightarrow \frac{I_{E^1}}{I_{E^2}} = \exp\left(\frac{V_{i1} - V_{i2}}{V_r}\right)$$

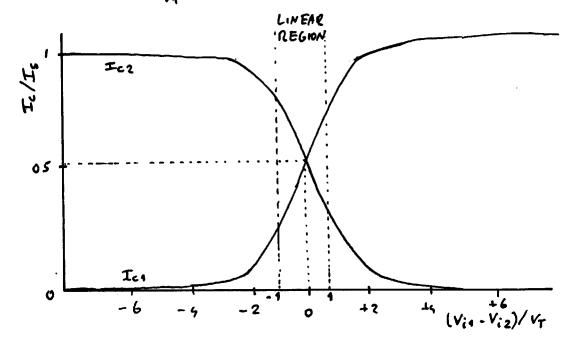
also: JE+ + JE2 = Is

$$T_{E1} = \frac{T_s}{1 + exp(\frac{V_{i2} - V_{i1}}{V_T})} \qquad T_{E2} = \frac{T_s}{1 + exp(\frac{V_{i1} - V_{i2}}{V_T})}$$

Assuming d=1 Ic. = IE1, I(2 = IE2

The resistances Rc are current-to-voltage translators

$$V_{04} = \frac{V_{cc} - \frac{R_c I_s}{1 + exp\left(\frac{V_{i2} - V_{i1}}{V_T}\right)}}{1 + exp\left(\frac{V_{i2} - V_{i1}}{V_T}\right)}$$



The amplifier is linear approximately for differential voltages not exceeding VT!

USE INPUT SIGNALS OF N 20 MV

CHAPTER 2

FREQUENCY RESPONSE

C4.7 Sedra

one of the most important parameters of electronic circuits is the frequency response. Normally we want as high a bandwidth as possible, but not always. Sometimes we want to cut off the DC part (for decoupling or to reduce power consumption or noise). Sometimes we want to limit the high-trequencies (to avoid oscillations). Sometimes both (bond pass amplifier).

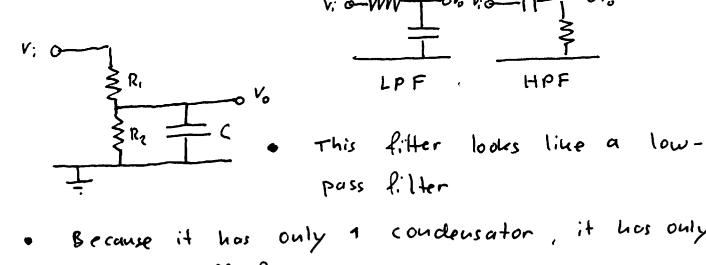
For advanced circuits (with many capacitors and inductors) the calculation is very complicated. The best thing is then to use electronics simulators such as Electronics Workbench an P-Spice.

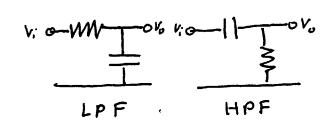
However, it is very usefull to get an idea of the forguency response. In order to do that

we will simplify our analysis. We will look for individual cut-off frequencies and then combine these in the final frequency response. Thus, the strategy becomes very simple:

Find filters like the LP and HP filters presented in Chapter O

As an example :





- · Because it has only 1 condensator, it has only one cut-off Prequency
- To find this Prequency we have to find the effective resistance this E sees. For this, we connect the input to ground and we get this

$$R_{1} \stackrel{\text{Reff}}{\rightleftharpoons} = R_{1} / / R_{2} \implies \omega_{0} = C (R_{1} / / R_{2})$$

$$\Rightarrow T(S) = \frac{A_{DC}}{1 + S / \frac{1}{(R_{1} / R_{2})C}}$$

The DC gain ADC can be found by considering the condensator as open-circuit:

$$A_{Dc} = \frac{R_2}{R_1 + R_2}$$

Thus

$$T(s) = \frac{R_2/(R_1+R_2)}{1+s/\frac{1}{(R_1/\!/R_2)}c}$$

with RillRz = RiRz // (Ri+Rz) this becomes

$$T(s) = \frac{1/R_1C}{s + 1/(R_1/R_2)C}$$
 (*)

The method we learned at Circuit Analysis results (of course) in the same:

Vi of This is a voltage divider with the impedance of a condensator as $\frac{1}{sC}$: $\frac{v_0}{v_i} = \frac{\left(\frac{1}{sC} / / R_z\right)}{\left(\frac{1}{sC} / / R_z\right) + R_1}$

$$\frac{v_{\bullet}}{v_{i}} = \frac{\left(\frac{1}{sc} // R_{z}\right)}{\left(\frac{1}{sc} // R_{z}\right) + R}$$

After some rearranging of terms the same (*) expression emerges. Try it.

Which method do you prefer?

Bode plots

As a Simplification of our analysis we will look for Simple filters in our circuit: Either LPF's or HPF's. In other terms, we will look for Single-pole (LPF) or Single-zero (HPF) filters, so-called first-orde functions. On basis of this we will draw a Bode plot observing the following rules:

- we start with a horizontal line (A=Ao)
- Every pole (LPF) introduces a cut-off frequency above which the slope is changed by -20 d8/dec.
- below which the slope is changed by +20 dB/dec

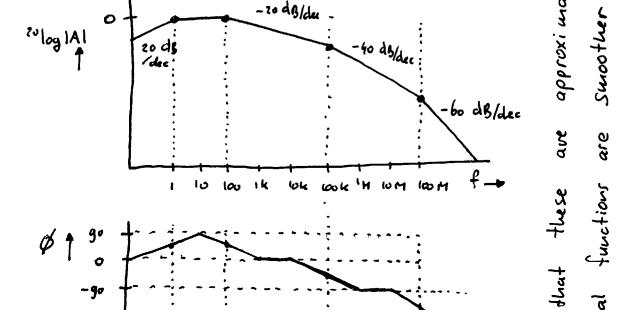
 At the phase plot:
 - · we start with oo
 - The phase changes -90° in approximately 2 decades (factor 100 in frequency) around the Cut-off frequency introduced by every pole (LPF). -45° before f_c , -45° after f_c . At f_c : $\Delta \phi = -45^{\circ}$
 - The phase changes $+90^{\circ}$ in approximately z decades around the cut-off frequency introduced by every zero (HPF). $+45^{\circ}$ before 4c, $+45^{\circ}$ dhr 4c. At 4c: $40 = 445^{\circ}$

Example:

what is the Bode plot of a filter (passive, Amone =1)

with theree poles (100 Hz, 100 KHz, 100 MHz) and one Zero (1 Hz)?

The mid band gain is 1 (with go'shill)



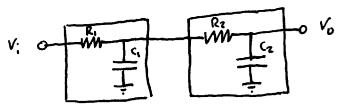
$$T(f) = \frac{1}{(1+jf/100)(1+jf/106)} \cdot \frac{1}{(1+jf/108)} \cdot \frac{1}{(1+jf/108)}$$

work

$$T(f)| = \frac{1}{\sqrt{f}} + \frac{1}{\sqrt{f$$

Bandwidth of filter: 100-1 = gg Hz This is a band-poss filter.

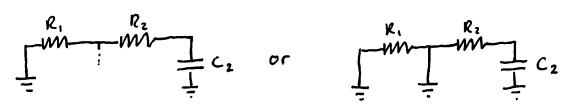
Warning 1: Don't he misled



what are the two poles of this filter?

simple thought: $\omega_1 = \overline{R_1C_1}$, $\omega_2 = \overline{R_2C_2}$ wrong!

For instance: we have to find the effective R that C_2 sees, while connecting V_i to ground. This might be $R_i + R_2$ (if C_i is considered open-circuit) or just R_2 (if C_i is considered Short-circuit). Which one is correct depends on values of R_i R_2 C_i and C_2 .

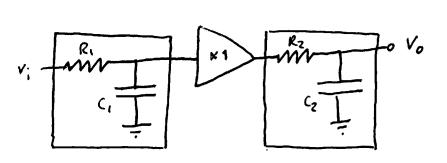


If the pole of filter 1 is much lower than that of the pole we are trying to find for filter 2 then we use the right circuit, because $f_2 >> f_1 \implies$ The first tilter is already blocking \Rightarrow G is effectively a short circuit. If the pole of filter 1 is much higher, then we use the left circuit and find $W_2 = (R_1 + R_2) C_2$

There are many ways to go to Rome. Many ways

Warning 2: multi pole /zero

Even if the individual filters are nicely decoupled, as in the ligure below, we have to be corelull.



note: ideal amplifier
(opamp) has

fin = 00, fout = 0

Imagine $R_1 = R_2 = R_{and}$ $C_1 = C_2 = C$. Two identical filters, what is the cut-off frequency of the total circuit? $W_1 = \frac{1}{RC}$, $W_2 = \frac{1}{RC} = W_1 = \frac{1}{RC}$? Wrong!

Remember: at the cut off frequency the amplitude is to of mid band amplitude, Per definition!

At $\omega = \omega_1$: $|T(\omega_1)| = \frac{1}{\sqrt{1 + \omega^2/\omega_1^2}} \cdot \frac{1}{\sqrt{1 + \omega^2/\omega_2^2}} = \frac{1}{2}$, be cause $|T(\omega)| = \frac{1}{\sqrt{1 + \omega^2/\omega_1^2}} \cdot \frac{1}{\sqrt{1 + \omega^2/\omega_2^2}} \Rightarrow \frac{1}{2}$

Easy calculation shows (w= w,):

$$|T(\omega_{tot})| = \frac{1}{v_2} \Rightarrow \frac{1}{1 + \omega_{tot}^2/\omega_i^2} = \frac{1}{v_2} \Rightarrow$$

 $\omega_{\text{tot}} = \sqrt{r_2^{1} - 1} \omega_1 \sim 0.64 \omega_1$

So, if, for instance, we link two 100 Hz LPF's together, the total cut-off frequency is 64 Hz. In the same way: for two VHPF's $w_{tot} = 1.55 w_1$

Normally what is interesting is to find the poss-bond. That is to say the lower and upper Prequencies of band that has a gain larger than it times the maximum gain. $f_L \cdots f_H$.

f_r ↓ H

When the individual lower cut-off
frequencies fer. free- for are well
seperated, or when at least the
higher one is well seperated, then
fr ≈ MAX (fli)

* The same accounts for the higher cut-off frequency for the well seperated")

fy = MIN (fui)

l'well seperated" weans more-or less a factor 4)
For instance:

 $f_{L4} = 1 \text{ Hz}, \quad f_{L2} = 2 \text{ Hz}, \quad f_{L3} = 2.4 \text{ Hz}, \quad f_{L4} = 30 \text{ Hz}$ $f_{H4} = 200 \text{ WHz}, \quad f_{H2} = 3 \text{ MHz}, \quad f_{H3} = 3.3 \text{ MHz}$ $\implies f_{L} \sim 30 \text{ Hz}, \quad f_{H} \sim 200 \text{ WHz}$

* when not well seperated it can easily be calculated as

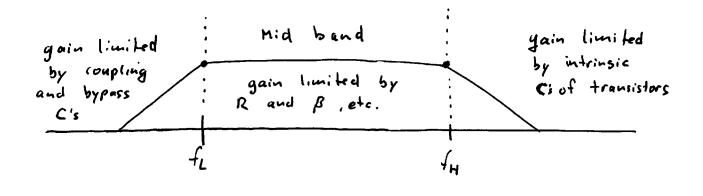
$$f_{L} \approx \sqrt{f_{L1}^{2} + f_{L2}^{2} + ... f_{LN}^{2}}$$

$$\frac{1}{f_{H}} \approx \sqrt{\frac{1}{f_{H_{1}}^{2}} + \frac{1}{f_{H_{2}}^{2}} + \frac{1}{f_{H_{3}}^{2}} \cdots \frac{1}{f_{H_{4}}^{2}}}$$

As can easily be verified these definitions reduce to the previous definitions for well seperated but-off frequencies.

In every textbook you can find a different approach. They are all approximations. It is more important to understand where the cut-off Trequencies are coming from — what is limiting the circuit—then to exactly know these frequencies.

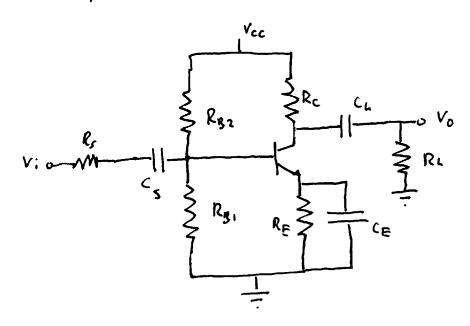
First design the circuit, then simulate it with SPICE. Then build it and test it in practice.



Frequency Response of the common - emitter amplifier:

we will now add (more) coupling condensators and a by pass condensator to our CEA.

The function of a coupling condensator is to remove the DC part of the input or output signal. The function of a byposs translator is to increase the mid band gain, as we will see, maintaining the blos polarization conditions.



CL, Cs: coupling

Capacitors

CE: bypass

Capacitor.

The capacitors Cs, CL and CE each introduce a lower cutoff frequency; they function as high-poss filters. For Cs and CL this is easy to see. Remember that a capacitor is short circuit for high frequencies and open - circuit for low frequencies. Why is CE also a high-pass filter?

Remember that the gain of a CEA is equal to the resistance at the collector divided by the resistance at the emitter. Thus

$$A = \frac{R_e}{R_E + f_e}$$
 and $A = \frac{R_c}{f_e}$
low frequencies high frequencies

Although this is not really a low-pass lilter (ADC #0), we can consider it as such.

bypass filter has a zero at f = 0 Hz and a pole at f = 0

For the law frequency behavior we thus have 3 filters. One determined by Cs, one by CL and one by CE. which one is domination. For Cs, should we consider CL and CE as open circuit or close circuit? (It will determine what effective resistance (s sees and what will be the cut-off frequency.) One trick we can use is the method of

SHORT - CIRCUIT TIME (ONSTANTS)

TO DETERMINE LOWER FREQUENCY

SHURT CIRCUIT TIME CONSTANTS METHOD Source to ground

⇒ Source to ground ⇒ Consider every other capacitor as short circuit (For instance, for Cs consider C∈ and CL as short circuit).

⇒ Determine ti = CiReffic for every capacitor in this way.

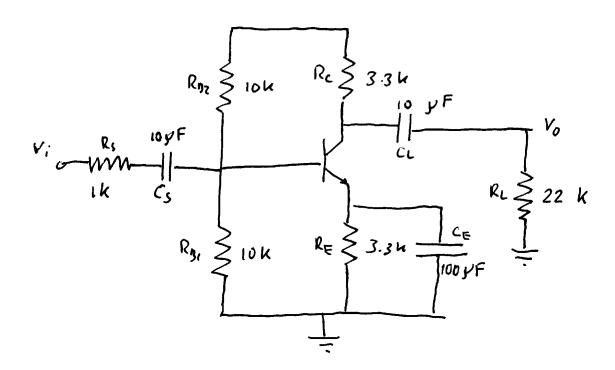
 $\Rightarrow \gamma_{\text{fot}}^{-1} = \overline{Z} \frac{1}{\gamma_i}$

 $\Rightarrow \omega_{L} = \frac{1}{\tau_{tot}} = \sum_{i=1}^{N} \frac{1}{\tau_{i}}$

FOR LOW FREQUENCIES

without proof: while this will not give correct results for the individual time constants, the final result for we is correct (p600 of Sedra).

As a byproduct, we will immediately see which capacitor is the limiting one.



Cs: Vs = 10yF. Reff . Reff : Short circuit all other (s:

$$R_{S} = \frac{1}{2} \sum_{i=1}^{n} \frac{1}{2} R_{g_{i}} = \frac{1}{2} R_{g_{i}$$

CE : TE = 100 yF. Reff

$$R_{g,1} = R_{g,2} \times R_{g$$

 $\gamma_{\rm E} = 100 \, \rm yF \times 20 \, \rm s^2 = 2.81 \, ms$ $(f_{\rm LE} = \frac{1}{277} = 56.7 \, \rm Hz)$

Ch. TL = 10 yF x Raff

fo ≈ \(\frac{V_A}{I_c}\) \(\tilde{\nu}\) 200 ksz

$$Reff = (f_0 // Rc) + RL$$

$$= (200 kz // 3.3 kz) + 22 kz$$

$$= 25.2 kz$$

$$T_L = (0yF * 25.2 kz = 0.25 s) (f_{LL} = \frac{1}{2\pi T_L} = 0.63 Hz)$$

Conclusions
$$C_{E} \qquad C_{S} \qquad C_{L}$$

$$P \qquad P \qquad P$$

$$T_{tot} = \sum_{i=1}^{N} \frac{1}{T_{i}} = \frac{1}{28 \, \text{ims}} + \frac{1}{24 \, \text{ms}} + \frac{1}{250 \, \text{ms}} \Rightarrow$$

$$T_{tot} = 2.5 \, \text{ms}$$

$$W_{L} = \frac{1}{T_{tot}} = 400 \, \text{rad/s} , \quad f_{L} = \frac{W_{L}}{2\pi} = 64 \, \text{Hz}$$

The bandwidth is limited by the capocitor giving the shortest time constant: CE.

If we want to increase the bandwidth, we should increase (E or decrease & (different transistor) or increase Rs.

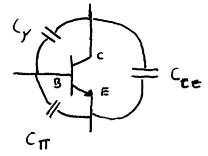
cr (t CE

High - frequency analysis

The high frequency response is normally limited by the intrinsic capacitonces of the transistors.

These capacitances are unavoidable and have a physical nature I see my option lectures "Physics of semiconductor

devices"). We can find the values for the capacitanas in the data sheets of the transistors used



capacitances of an upa transister

Cy is capacitance between collector and base

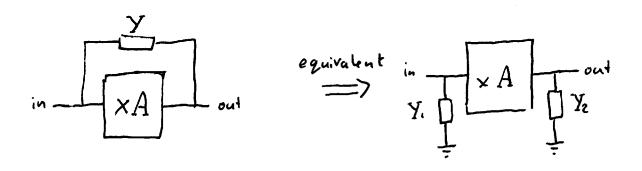
LTT is capocitance between bace and emitter

Cce is copacitance between collector and emitter and is normally emitted from the calculations.

Examples: G= 15 pf. G= 10 pf

To find the upper cut-off frequency fix we have to find the effective resistance these capacitors see. However, there is a complication: The capacitors are connected to both the input and the output. For instance cy is at the input (ve) and the output (ve) of the transistor. This causes feedback (see next chapter). We can analyze it if we use Miller's theorem

Miller's Theorem



An admittance Y (for instance C, Lor 1/2)
bridging part of a circuit with voltage gain A
can be decomposed into a circuit with an admittance
at the entrance (Y,) and at the exit (Yz) of the amplifier.

$$Y_1 = Y(1-A)$$

$$Y_2 = Y(1-A)$$

The admittance is amplified at the entrance and reduced (slightly) at the exit.

How can this be? Take the example of a capacitor C bridging an amplifier with 100 x gain. The capacitance that is felt at the entrance is the charge that is stored in the capacitor. By delinition:

$$C_{\text{eff}} = \frac{dQ}{dV}$$

example C= inF A =-100.

0V | X-100 | 0V | 0ut 0

At OV at entrance: the exit voltage is also ov and the capacitor is empty

$$Q = \Delta V C = (V_{in} - V_{out}) \times InF = O C.$$

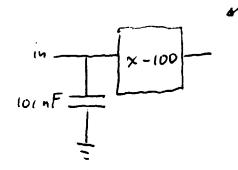
Let us increase it to 1 V at the entrance and see how much charge will be in the capacitor, with a gain of -100 there will be -100 V at the other side. The amount of charge in the capacitor is then

Q = AV-C = (1-(-100)) x in F = 101 nC

Seen from the entrance, it looks like a capacitor total charge

$$C = \frac{Q}{IV} = \frac{101 \text{ nC}}{IV} = 101 \text{ nF}$$
Imput signal

in other words, at the input it looks like the figure

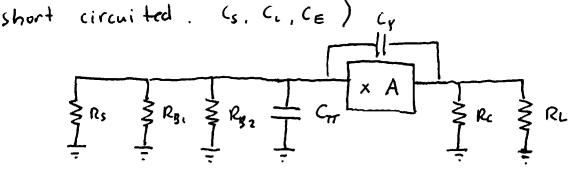


For other types of admittance we can make a similar admittance to summary:

capacitanus are multiplied at entrance. Resistances on reduced Note that we can only use Millers theorem when the admittance does not (significantly) change the gain. It can (therefore) also not be used to determine the input and output resistances of the amplifier.

The effect on the capacitances is called the miller effect and this influences the high-frequency response of the amplifier.

We will consider the two capacitors Cy and Cy. They will cause low-pass filters
As the circuit we have (note: all other capacitors



1 MILLER

$$\begin{cases} \mathcal{L}_{g_1} & \begin{cases} \mathcal{L}_{g_2} & \frac{1}{2} & (-A)\zeta_{g_2} & \frac{1}{2} & (-A)\zeta_{g_2} & \frac{1}{2} & \frac{1}{2$$

The voltage gain A from the entrance to the exit of the transistor (base - to - collector, where the capacitor is connected) is (note: Re is bypassed)

$$A = -\frac{(R_c//R_l)}{r_e} = -\frac{(3.3 \text{ kg.} // 22 \text{ kg.})}{20 \text{ s2}} = -143$$

(note the trumendous effect in gain caused by by possing RE. From $\alpha - 1$ to $\alpha = -143$)

Now we can calculate the time constants:

= 1220 ns
$$(f_{Hin} = \frac{1}{2\pi T_{in}} = 130 \text{ kHz})$$

[note: the "Miller effect" for C_{Π} is 1, because the "gain" from base to emitter is 0 (emitter is connected to ground), thus $C_{\Pi} = (1-A)C_{\Pi} = (1-0)(\pi = C_{\Pi})$

= 2.87 ks. 10.07 pF

There are thus two low-pass filters. One with a time constant of 1220 ns and the other with

In case the individual cut-off frequencies are not well seperated, we can use the trick of

OPEN - CIRCUIT TIME CONSTANTS

TO DETERMINE HIGHER CUT-OFF FREQUENCY

⇒ source to ground

=> for every capacitor causing a LPF, consider all other capacitors (of LPF's) as open circuit.

=> Retermine ti for every capacitor in this way

 \Rightarrow $\tau_{tot} = \sum \tau_i$

 $\Rightarrow \qquad \omega_{H} = \frac{1}{t_{40+}} = \frac{1}{\sum t_{i}} \qquad f_{H} = \frac{1}{2\pi} \omega_{H}$

In this case we would find

Ttot = tin + tout = 1280 ms + zy ms = 1249 ms

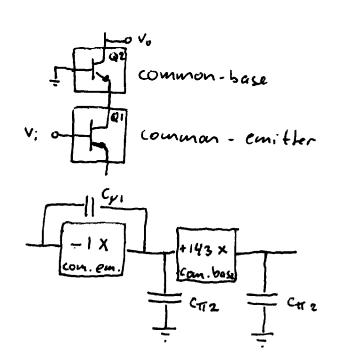
 $W_{14} = \frac{1}{1249 \text{ ns}} = 8.0 \cdot 10^6 \text{ rad/s}$

fit = 127 KHZ (compore to dominat-pole technique)

frequency, this is exact

As we will see in the practical lectures, the sollution to this is the coscode amplifier.

A cascode amplifier is a common-emitter amplifier in series with a common-base amplifier

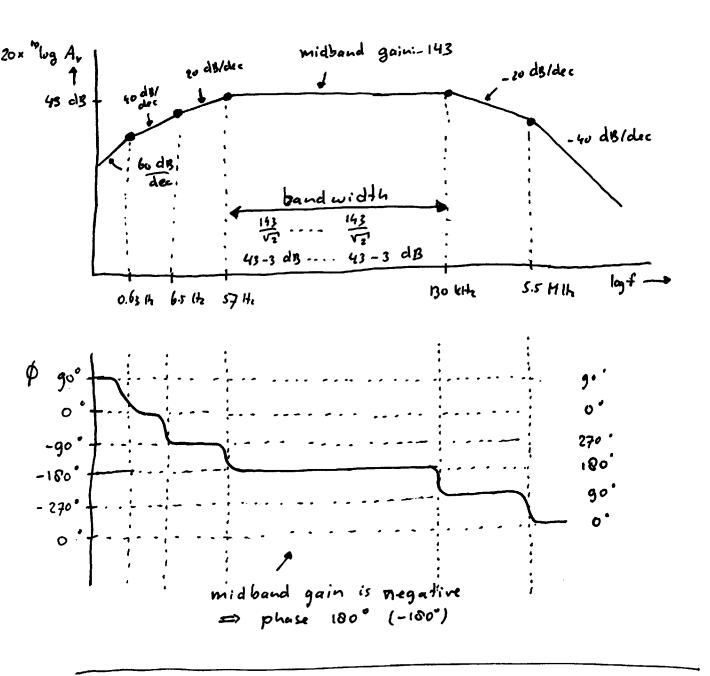


The gain of the Common emitter is -1, because it is $-\frac{r_{e2}}{r_{e1}}$. The Miller effect is reduced to only a factor 1-(-1)=2.

The common - base stage has a high gavin $\left(+\frac{Rel/Ri}{r_{e2}}\right)$

but because the base is connected to ground, the Miller effect has disappeared (=1). Only CT2 at input and output.

Summary / Bode plot of the CEA



At the practical lessons we will further study the frequency response of the differential pair of chapter 1. (For more information, see Sedra's chapter 7.8)

CHAPTER 3

FEEDBACK

ch. 8 of Sedra

Feedback is the concept of putting part of the output signal back at the entrance input of the amplifier or circuit.

There are various advantages to this:

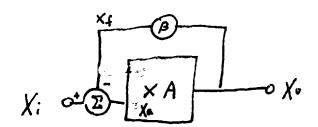
- * stabilize the gain (independence on B, etc)
- * change output and input resistances
- * extend the bandwith

There are also negative effects such as

+ instability (oscillations)

The basic feedback circuit consists of an amplifier, with a gain A and a feedback loop, which put part, A, of the output back at the input. For negative feedback this is subtracted

at the input:



(We consider here only <u>negative</u> feedback.

It is not so difficult to see that positive feedback results in a runaway signal).

For negative feedback like in the figure above, it can be shown that

 $(1) \qquad \chi_0 = A \chi_{\alpha}$

(X can be voltage or current!)

 $(z) \qquad xt = \beta x^{\circ}$

(3) $X_{\alpha} = X_{i} - R_{f} = X_{i} - \beta X_{o}$ (3) into (1):

$$x_o = A(x_i - \beta x_o)$$

$$\frac{X_o}{X_i} = \frac{A}{1 + A\beta}$$

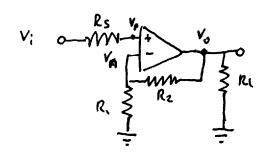
NEGATIVE FEEDBACK

Ap is called the loopgain

When the amplifier A is an ideal amplifier, $A = \infty$ and the amplification becomes $\frac{X_0}{X_1} = \frac{1}{B}$

This is an interesting result; the gain of an ideal amplifier with feedback is determined by the feedback loop.

Operational amplifiers have very large gain lot the order of 105) and the gain of op-amp's is therefore controlled by the feedback. As an example



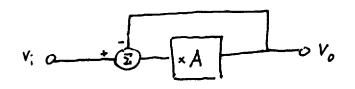
The feedback is from vo to vo and is supplied by a voltage divider R., Rz:

$$\beta = \frac{R_1}{R_1 + R_2} = \frac{1 \, \text{kr}}{1 \, \text{ks} + 10 \, \text{ks}} =$$

- · The open-loop gain is the gain from v; to Vo, with the feedback disconnected. This is thus 104
- Because $V_{in} = \infty$, $i_i = 0$ and $V_p = V_i$

$$V_i = \frac{A}{V_0} = \frac{A}{V_0}$$

In the other extreme case, when the amount of feedback is 100%



In this case the gain is

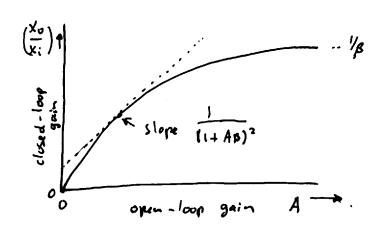
$$\frac{v_o}{v_i} = \frac{A}{1+AB} = \frac{A}{1+A} \approx 1$$

The voltage at the output is exactly the voltage at the input. For this it is called a tension-follower the advantage is that it can convert a circuit with high output resistance into a circuit with low output resistance. (Imagine connecting 8 52 speakers to our differential pair).

Desensitizing the gain. Not all amplifiers lopamps)
coming from the lactory are equal. They all have
slightly different gain. Typically in the order of 5%.
For some applications this is not accurate enough.
The gain can be stabilized by feedback

$$\frac{d\left(\frac{\sqrt{a}}{x_i}\right)}{dA} = \frac{1}{\left(1 + A\beta\right)^2}$$

$$\frac{d\left(\frac{x_o}{x_i}\right)}{dA\left(\frac{x_o}{x_i}\right)} = \frac{1}{(1+A\beta)^2} \frac{A}{(1+A\beta)}$$



The <u>relative</u> change in gain is thus related to the relative regain of the open circuit:

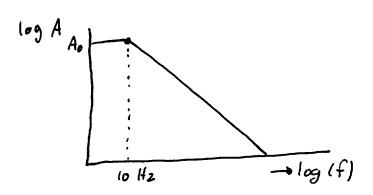
$$\frac{d\left(\frac{x_0}{x_i}\right)}{\left(\frac{x_0}{x_i}\right)} = \frac{dA}{A} \times \frac{1}{11+A\beta}.$$

Thus, the variations of different amplifiers is reduced by a factor $\frac{1}{1+A\beta}$. The gain is much more stable than the open circuit amplifier. An "error in gain of the amplifier of $\frac{dA}{A} = 5\%$ has only a relative error of $\frac{1}{1+A\beta}$. 5% in the final circuit. The price that is payed is a reduced gain:

From A to $\frac{A}{1+A\beta}$

Bandwidth extension

An amplifier with feedback has an increased band width. As an example, take a typical op-omp.



with a cut-off frequency at 10 Hz. The transfer function of this is

$$A(s) = \frac{A_o}{1 + s/\omega_o}$$

$$\omega_{e} = 2\pi \times 10 \text{ Hz}$$

$$Ao = 10^{5} (4ypical)$$

using this op-amp in an amplifier with feedbake

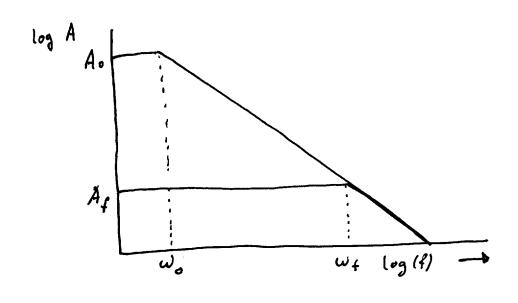
$$A_f(s) = \frac{A(s)}{1 + A(s)\beta} = \frac{A_o/(1+5/\omega_o)}{1 + A_o\beta/(1+5/\omega_o)}$$

$$= \frac{A_o/(A_o\beta+1)}{1+S/(\omega_o(1+A_o\beta))}$$

In other words:

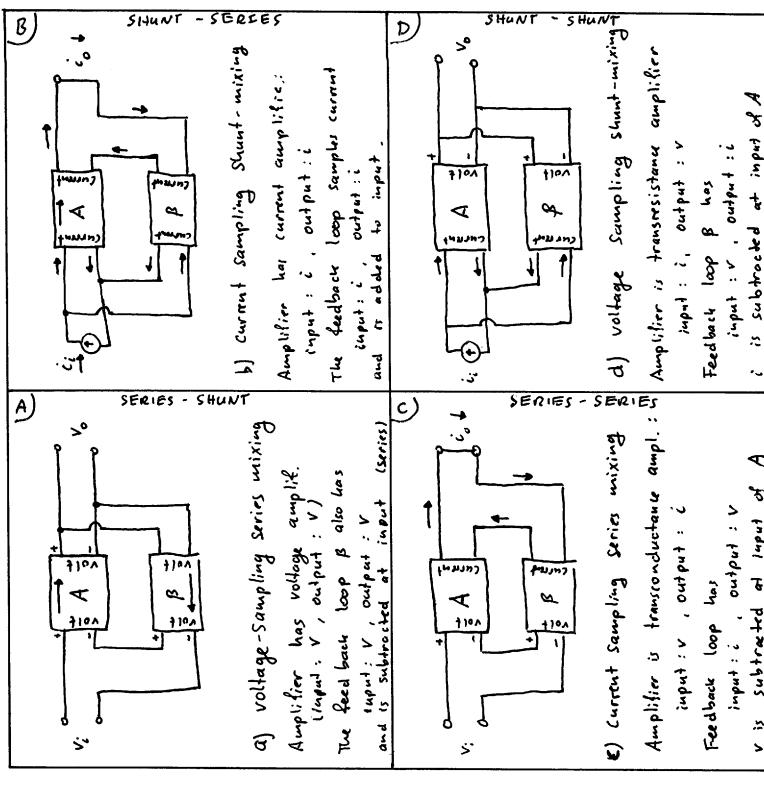
and the new cut-off frequency is $\omega_f = \omega_0 (1 + A_0 \beta)$

By using feedback, the bandwidth of the amplifier is increased. The price that is payed is a reduced midband gain $A_0 \rightarrow A_f = \frac{A_0}{1+A_0B}$



Topologies

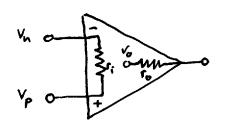
In the examples we used above, the output of the amplifier was a voltage signal and this was partially fed-back with a factor β and added to the input as a voltage signal. This topology is called voltage-Sampling series-unixing (A)



amplifier the is The Where a ex treme is with ampli fier Sampled current is This and a • at factor subtracted (B) the input of current mix tures and topologies 44 an two (r -i) has a transconductance amplifier voltage , (c)

Output Resistance

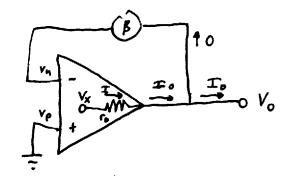
The input and output resistances of the amplifier also change significantly. This is best illustrated on basis of an operational amplifier



ri: input resistance

ro : output resistance

To determine the effect on the output resistance we consider the input resistance infinite and connect (for the "inventing amplifier) Vp connected to ground.



Because fi = co Ino current goes to vn)

$$V_{x} = -A V_{n}$$

$$V_{0} = V_{x} - I_{0} r_{0}$$

$$V_{n} = \beta V_{0}$$

substituting gives

$$T_o = V_o \frac{1+A\beta}{\Gamma_o}$$

with the definition of output resistance

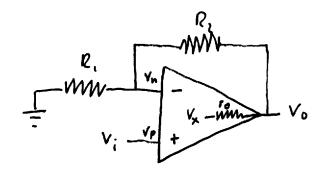
$$\Gamma_0 = \frac{1}{\partial V_0}$$
 we get
$$\Gamma_{0f} = \frac{\Gamma_0}{1 + A\beta}$$

In other words: the output resistance is reduced by a factor 1+ AB by using feedback.

Since the amplifier is a linear circuit, for other voltages at the input (Vp) we will find the same result.

In the above example a feedback that is not loading the output was assumed. Normally the feedback loop is made with resistances and other conductive elements. In this case, there is a current being drawn from the output of the amplifier. When this amplifier has zero andput resistance, the effect is nil; the amplifier can easily supply the current. If the output resistance to of the amplifier is not zero there is an effect on the open loop gain A.

As an example: assume ro to:



$$\beta_0 = \frac{R_1}{R_1 + R_2}$$

$$\frac{V_0}{V_i} = \frac{A}{1 + AB} \leftarrow ideally (r_0=0)$$

$$\frac{V_x}{V_i} = \frac{A}{1+A\beta'}, \quad \beta' = \frac{R_1}{R_1+R_2+r_0}$$

$$\frac{V_0}{V_i} = \frac{V_X}{V_i} \cdot \frac{V_0}{V_X} = \frac{A}{1 + \frac{R_1}{R_1 + R_2 + r_0}} A \qquad \frac{R_1 + R_2}{R_1 + R_2 + r_0}$$

$$= \frac{Ad}{1 + Ad\beta_0} \quad \text{with } d = \frac{R_1 + R_2}{R_1 + R_2 + \Gamma_0}$$

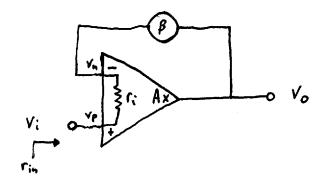
$$\beta_0 = \frac{R_1}{R_1 + R_2}$$

In other words: because of the current loading of the feedback loop ($R_1+R_2<\infty$) and the non-zero output resistance ($r_0\neq o$) the open-loop gain is reduced to

$$A_1 = A \cdot \frac{R_1 + R_2}{R_1 + R_2 + \Gamma_0}$$

Input Resistance

The input resistance can significantly increase when feed back is used



In this case it can be shown that:

$$V_o = (V_P - V_n) A = (V_i - V_n) A$$

$$V_n = \beta V_o = A\beta (V_i - V_n)$$

$$V_n = \frac{AB}{1+AB} V_i$$

$$\frac{T_{i} = \frac{V_{p} - V_{n}}{\Gamma_{i}} = \frac{V_{i} - \frac{A\beta}{1 + A\beta} V_{i}}{\Gamma_{i}} = \frac{1}{\Gamma_{i}} \cdot \frac{1}{1 + A\beta} \cdot V_{i}$$

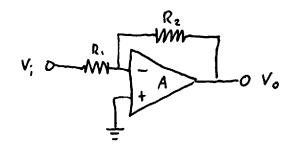
$$\Gamma_{in} \equiv \frac{1}{\partial V_i} = \Gamma_i (1+AB)$$

Because of the feedback, the input resistance of this amplifier has increased a factor 1+AB.

Not always is the increase in input resistance

so dramatic

Example: Inventing amplifier with negative feedback.

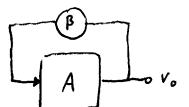


- a) what is the gain $(A_r = \frac{V_o}{v_i})$ of this circuit?
- b) what is the output resistance?
- c) what is the input resistance?

$$(Ausw: -\frac{AR_2}{AR_1 + (R_1 + R_2)}, r_{out} = \frac{r_o}{l + AB}, r_{in} = R_1 + \frac{R_2}{l + A})$$

Feedback and Stability / oscillators

One of the negative aspects of feedback is that it can induce instabilities loscillations) in the Signals. This means that we can have an output signal at a certain frequency without having any input signal connected. It is clear that passive circuits luithout amplification in any point) cannot oscillate, because the energy needed has to come from comewhere.



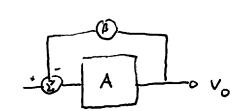
Generally speaking, a circuit

A lovo with feedback & and open-loop gain A will oscillate when

AB = 1. This is the Bark hausen [Criterion]

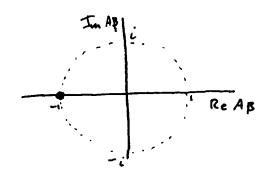
For this case, any voltage at input of amplifier is added with factor 1 at amplifier and added again ... ab infinito! The output signal will be infinite. Note that often A and B depend on frequency. So it can occur that the output will be infinite for only certain frequencies It will oscillate for all tregumnies at which Alf). P(f) = 1

For our amplifier with negative feedback found a gain of $\frac{x_0}{x_i} = \frac{A}{1 + A\beta}$ we found a gain of



Also here we can see that if $A\beta = -1$ then the output will be infinite for any tiny voltage at input. Normally, noise is present at any point of the circuit (~ yv. mv) and this will initiate the oscillations.

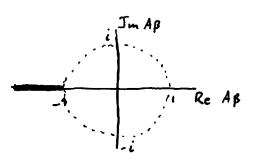
 $A\beta = -1$ is equal to saying $|A\beta| = 1$ and the phase $\angle AB = 180^{\circ}$, or in a phase diagram



← The • gives the Barkhausen Criterion for amplifiers with negative feedback The --- represents the points where IABI = 1.

using the same reasoning (positive feedback): If the loopgain AB>1, also oscillation will occur. For instance, for $A\beta = 2$ and starting with LyV at the entrance, this voltage is fed back to the entrance with a factor 2 and added. Now we have 3 pV at entrance. Then $3+6 \text{ pV} = g \text{ pV} \cdots \text{ etc.}$

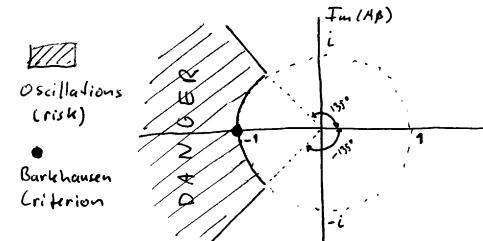
In our picture of negative feedback:



Oscillations when |AB| > 1 $\angle AB = 180^{\circ}$

See ____

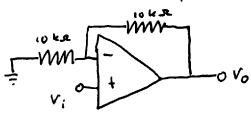
Finally, a good electronic designing proctice is to allow for a phase margin in the design. Normally 45° is used. With this, the final Nyguist plot (Im (AB) v.s. Re (AB)) becomes



Negative feedback.

Relaß) Nyguist plot.

As an example



An op-amp with negative feedbakk.

A has two poles, to Hz and

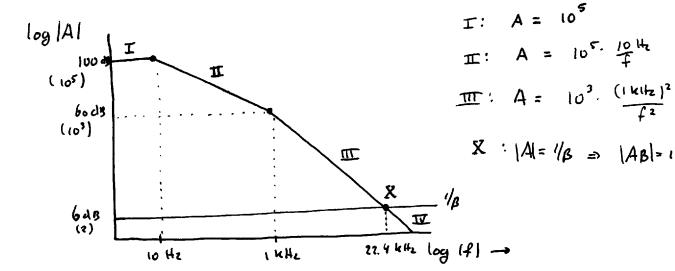
I KHz. The DC gain is +105, Will

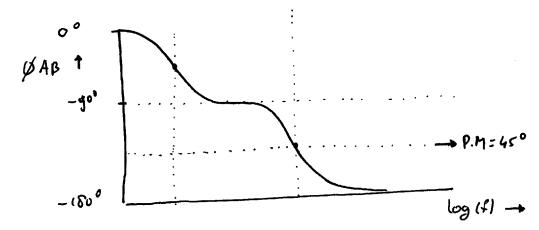
this circuit oscillate? If so, at

what frequencies? Assume rin = co, ro = 0, P.M. = 450

$$\beta = \frac{R_1}{R_1 + R_2} = 0.5 \quad \psi = 0 \implies \phi(AP) = \phi(A)$$

$$1/\beta = 2$$





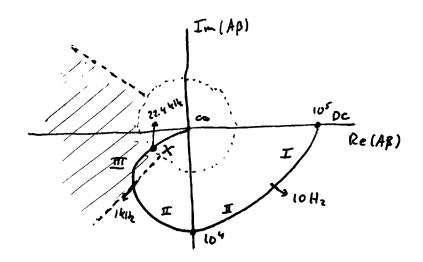
- When carrie of IAI crosses (arve of 1/BI:

 IABI=1, we are somewhere on the circle in the

 Nyguist plot. But where?
- when $1A1 < 11/\beta 1$, the we are inside the circle and here the circuit is stable. Zone IV
- In zones I and II, the phase is between 0° and -135° and the circuit is Stable
- the problem is in zone III. Here the loop gain lApl is still larger than 1 and the phase is

in side the danger zone.

In a Wyquist plot:

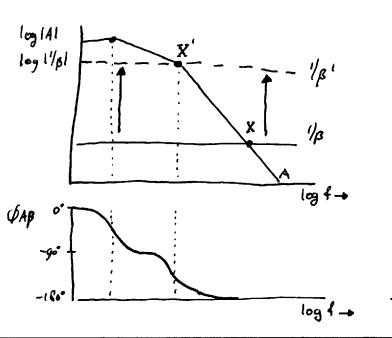


conclusion: The circuit runs the risk of oscillating in the frequency range 1 kHz - 22.4 kHz

The oscillations caused by feedback are not always bad. In fact, we can make oscillators in which the drequency is designed

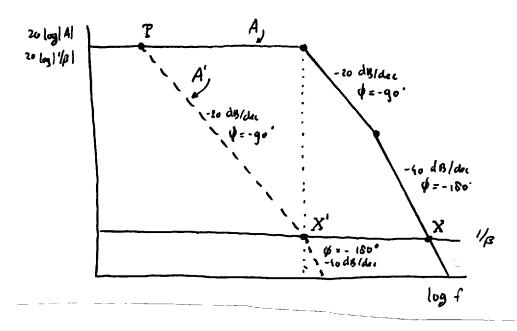
How can the above circuit be stabilized?

1) we could reduce the amount of feedback ?



Marginally Stuble: $X': |A\beta|=1$, $|A\beta|=-(35^{\circ})$ $(P.M=45^{\circ})$ Re AB It is not difficult to show that a $\beta=10^{-3}$ is needed to Stabilize the circuit. For example with $R_1=100$ s and $R_2=100$ ks.

Frequency compensation is another method for stabilizing the circuit, although it is rather done in the factory of the opamps. It consists of introducing a new pole in the open-loop gain A.



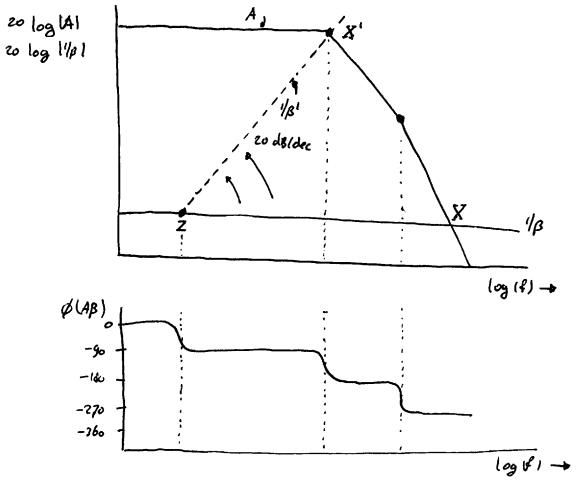
In the above figure: by introducing a new pole P at low frequencies the gain is reduced to below 1/3 before the phose changes of the other poles take effect. To be sure this works for any B, a B of 1 has to be used in the calculation for the design of P

Most modern op-amps implement this dechnique und have extremely low cut-off frequencies (at around 10 Hz).

Question: what would be the frequency of the pole P needed in our op-amp in order to stabilize it for $\beta=0.5$ and for $\beta=1$ (answers: 2×10^{-9} Hz and 1×10^{-9} Hz)

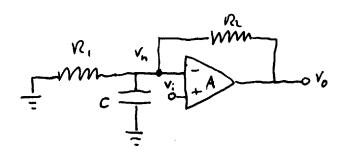
3 External compensation

In a similar way, introducing a pole in B (a zero in 1/B) will result in Stabilization of the circuit



By the zero z, the 1/8 is pushed up to make it cross with A earlier, before the first pole of A.

The idea is to put an LPF in the feedback circuit B. For Instance:



It is not difficult to see that

$$\beta = \frac{v_n}{v_o} = \frac{R_1/(R_1+R_2)}{1+(R_1/R_2) s C} \longrightarrow DC \quad gain = \frac{R_1}{R_1+R_2}$$

$$cut - off \quad frequency$$

$$\frac{1}{2\pi T(R_1/R_2) C}$$

which we could have directly seen by considering the effective resistance seen by C, with vo and vi connected to ground.

Question: what will be the capacitance (needed to stabilize our circuit of page 16? (Answer: fc = 2 x 10-4 Hz, C = 160 mF)

CHAPTER

4

OPAMP CIRCUITS

The operational amplifier is a very versatile component that can be used in many ways, ranging

- · high gain amplifiers
- · active filters
- · Signal generators
- · comparators
- · Schmitt triggers
- · tension followers



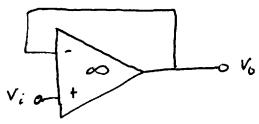
· current controlled voltage sources.

An	i deal	орашр	has			
	1)	indinite	gain	, A = 03		
	2)			resistance	$f_i = \infty$	
	3)	Zero	out put	resistance	r _o = 0	
L				_	_	

1a) Because
$$A = \infty$$
, $V_p - V_n = V_0 / A = 0$

$$\implies V_p = V_n !$$

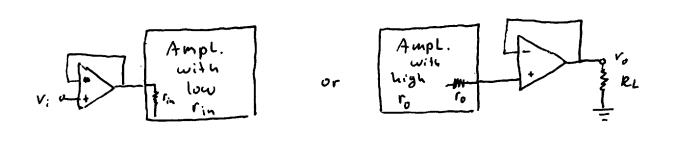
The easiest circuit we can make with an op-amp is a Itension follower:



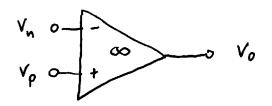
with 100% feedback ($\beta=1$) and assuming an infinite open-loop gain ($A=\infty$) it is easy to show that $V_0=V_1$.

The advantage of this circuit is that it has very high input resistance and low output resistance.

This is usefull when we cannot load a high-ohmic source or when we need to drive a low-ohmic input stage.

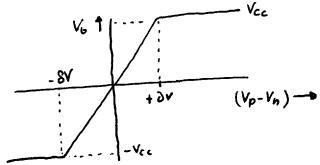


A <u>Comparator</u> is a circuit that has either V_{cc} or $-V_{cc}$ (the supply voltage) as output, depending on the difference in the input terminals.



$$V_0 = -V_{cc}$$
 if $V_p > V_n$

For op-amps with non-infinite gain A, there is a region of input vollages that don't give ± Vcc at the output

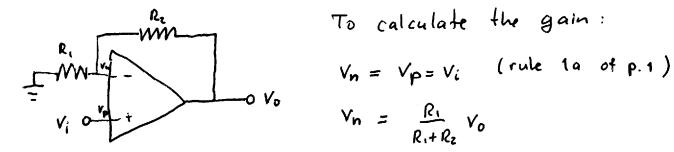


It is easy to show that DV = Vcc/A and is of the order of 10 V/105 ~ 100 yV for practical opamps.

A widely used Comparator opamp is the "311" which has a high switching speed -Vcc + Vcc

A [non-inverting amplifier] can be made by

introducing (negative) feedback to the amplifier.



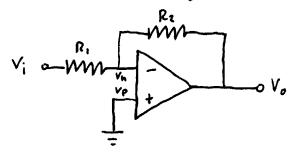
To calculate the gain:

$$V_n = V_p = V_i$$
 (rule 1a of p.1)

$$V_n = \frac{R_1}{R_1 + R_2} V_0$$

$$\implies \frac{V_0}{V_i} = \frac{R_1 + R_2}{R_1}$$

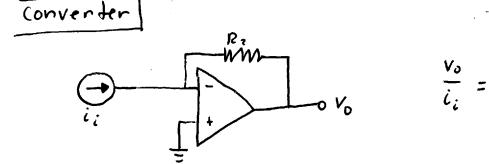
An inverting amplifier is equal to the one above, but with the signal connected to Ri:



 $V_n = V_p = 0$ V and that is why the negative terminal in this scheme is often called <u>virtual ground</u>. A current of $I_i = \frac{V_i}{R_i}$ is drawn from the source and (since $r_{in} = co$), this current must go through R_2 . The output voltage thus becomes

$$V_0 = \frac{R_2}{R_1} \cdot V_i \implies \frac{V_0}{V_i} = \frac{R_2}{R_1}$$

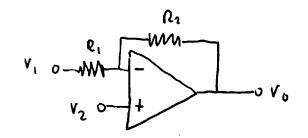
The same idea is also va [current-to-voltage



$$\frac{v_o}{\dot{c}_i} = R_z$$

For a [differential amplifier] we connect

both inputs:



using superposition we can easily see that

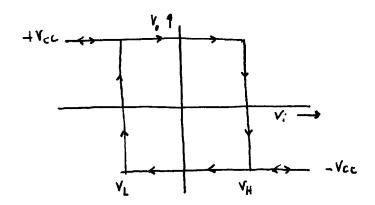
$$= \frac{R_2}{R_1} V_2 - \frac{R_1 + R_2}{R_1} V_1 \approx \frac{R_2}{R_1} (V_2 - V_1) \quad (for R_1 << R_2)$$

we have to always bear in mind that a high gain for $R_2 >> R_1$ (β is very small) will limit the band-width. See $\rho.7$ of chapter 3:

with fo the open-loop bandwidth and Ao the open-loop gain. In fact, the gain-bandwidth product.

is constant
$$\left(\frac{v_o}{v_i} = \frac{A}{1+AB}, f_c = f_o(1+AB)\right)$$
 $GBW = Af_o$

SCHMITT TRIGGER is like a comparator, but it has a memory. The output of the schmitt trigger not only depends on the input voltage, but also on the history.



To achieve positive feedback is used

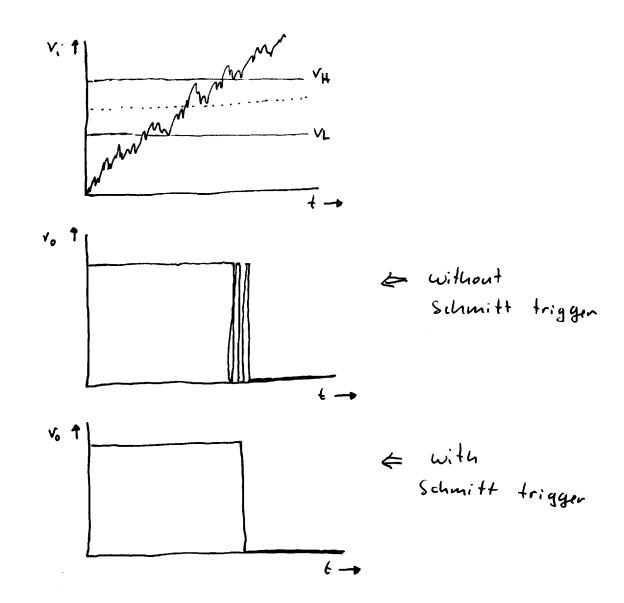
$$V_{\rho} = \frac{R_{1}}{R_{1} + R_{2}}, V_{o}$$

If $V_0 = +V_{CC}$, then $V_P = +\frac{R_1}{R_1+R_2}V_0$. Now, if we increase V_i from -co upwords, there comes a point where $V_i > V_P$ and thus, since the circuit works as a comparator, V_0 becomes $-V_{CC}$. This makes $V_P = -\frac{R_1}{R_1+R_2}V_0$. To make the output commute again, we have to lower V_i to this value.

$$V_{L} = -\frac{R_{1}}{R_{1}+R_{2}} V_{CC}$$

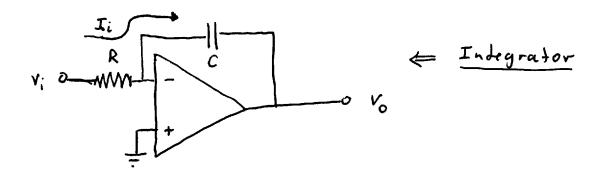
$$V_{H} = +\frac{R_{1}}{R_{1}+R_{2}} V_{CC}$$

The advantage of a Schmitt trigger lies in the fact of eliminating noise.



Imagine switching on the lights in a room based on a detector.

Integrators and Differentiators are made by putting a condensator in the feedback loop.



The resistor translates the voltage to a current Li = Vi/R. This current cannot enter the opamp and thus is used to charge the Capacitor C. The amount of charge in C (assuming at t=0 discharged, Q(t=0) = 0) is equal to the integrated current:

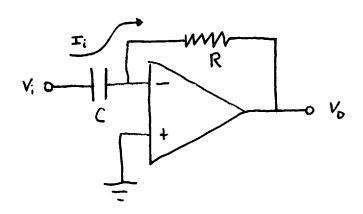
$$Q(t) = \int_{0}^{t} I_{i}(t) dt = \int_{0}^{t} \frac{V_{i}(t)}{R} dt$$

The voltage drop induced by this charge is

$$\Delta V_c = Q/C$$

since one side of the capacitor is connected to virtual ground, the voltage drop is equal to -Vo. Thus

To make a differentiator, we exchange the resistance and capacitor



The input current Ii is equal to $I_i = C \cdot \frac{dv_i}{dt}$

This current is translated to voltage by R (note that one side of the resistor is at virtual ground and the input resistance of the op-amp is infinite; all current goes through R).

$$V_{o}(t) = -CR \frac{dv_{i}(t)}{dt}$$

In both cases, the differentiator and integrator the signals at the output might be limited by the power supply. Vo cannot be larger that $\pm V_{CC}$. In the case of the integrator it means that, for instance, DC signals at Vi can only be integrated up to a certain time. For the differentiator it means that signals cannot change too fast.

with the integrator and differentiator circuits we can build analog computers. For instance for solving differencial equations.

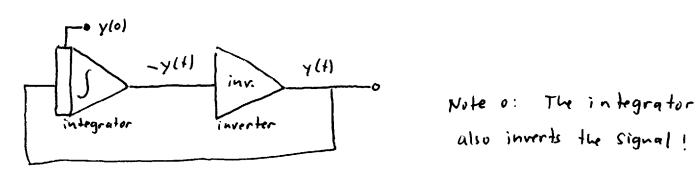
Take for example the differential equation

$$\dot{y} = y$$
 with $y/0) = 1$ $\left(\dot{y} = \frac{dy}{dt}\right)$

This is equivalent to (integrating on both sides)

$$y(t) = y(0) + \int_{0}^{t} y(\tau) d\tau$$

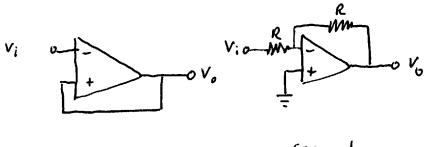
with our op-amp circuits this becomes



also inverts the signal!

Note 1: the 10 y(0) part is to load the inverter with the storting value 1 implies charging the capacitance instantaneously).

Note 2: The inverter can also easily be made of opamps. Why is it not the left circuit?



wrong

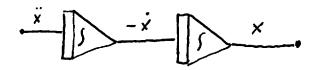
correct

As another example:

$$\ddot{X} + 0.5\dot{x} + X = 4.0 \qquad x(0) = 0 , \quad \dot{x}(x) = 1$$

$$\dot{x} = \frac{dx}{dt}, \quad \ddot{x} = \frac{d^2x}{dt^2}$$

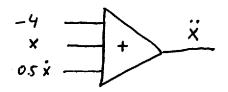
1) Storting with assuming & exists:



2) Rearrange the equation

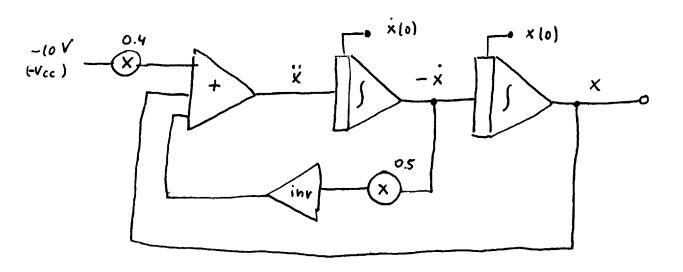
$$\dot{x} = -0.5 \dot{x} - x + 4.0$$

This is equal to

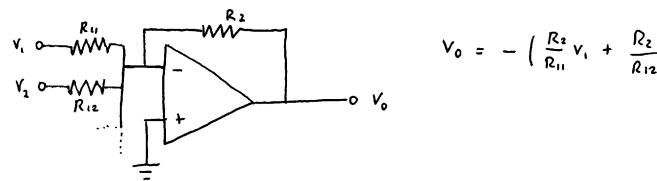


(The summing opamp also inverts!)

3) Now connecting the two parts ("procedurs")



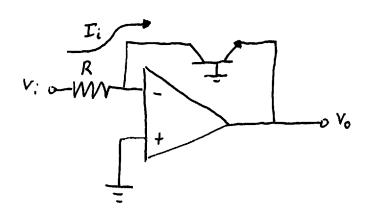
- * The multipliers & are easily made with opamps. when it is a constant multiplication factor.
- * The adder +> can also be made with opamps.

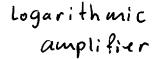


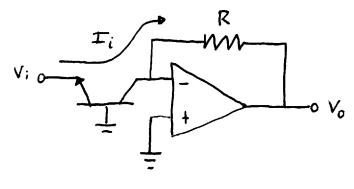
* The circuit on the previous page can be simplified because there are too many inventors, but this is a small detail.

The circuit on the previous page is an example of how a damped oscillation can be calculated using analog electronics. An example of a damped oscillation is a guitar String or a bell. Thus, the above circuit generater musical Signals. The first electronic synthesizers were made in this way. We can imagine that the values at Γ $\dot{x}(0)$ and Γ x(0) were put there by a touch of a key, where the note (frequency) is also determined by the integration (onstants (RC) of the integrators.

Other "mathematical" circuits are the exponential and logaritmic amplifiers







exponential amplifier

$$T_c = \frac{V_i}{R} = T_o \left\{ e_{XP} \left(\frac{V_{BE}}{V_T} \right) - i \right\}$$

Ignoring the -1 and using $V_0 = -V_{RE}$ we see that

$$V_o = -V_T \ln \left(\frac{V_i}{I_o R} \right)$$

Note that Vo has to be positive.

For the exponential amplifier it is not difficult to show that

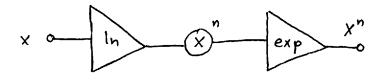
$$T_i \approx -T_0 \exp\left(-\frac{V_i}{V_T}\right)$$

$$V_0 = -T_i R = T_0 R \exp\left(-\frac{V_i}{V_T}\right)$$

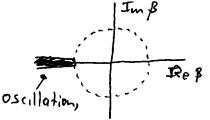
(note: V: has to be negative)

Combining logarithmic and exponential (anti-logarithmic) amplifiers we can make calculations of the type

$$y = \exp(n * \ln(x))$$

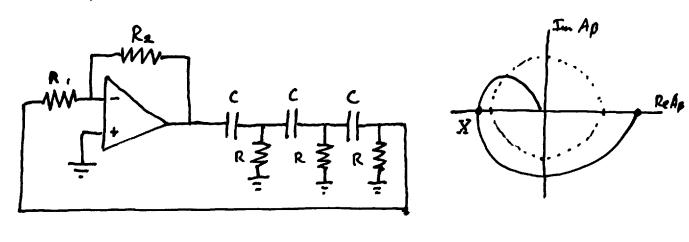


Oscillators In chapter 3 we saw how to avoid oscillations. Now we will use the same analysis to make oscillations happen. We need



Ap to become real and <-1 for some frequency (see Nyquist plot here). Assuming a flat A, without poles and phase changes, we can see that 3 poles are needed in B to achieve that.

For example

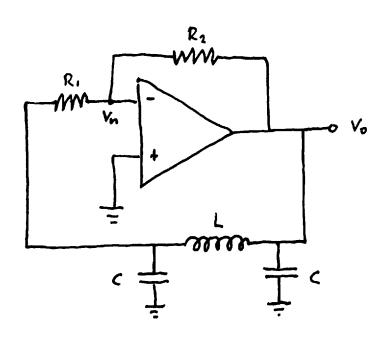


$$\beta = \frac{R^3}{(R^3 - 5R/\omega c) + j \left(\frac{1}{\omega c} - 6R^2/\omega c \right)}$$

In the oscillation frequency, at X, the imaginary part of β is zero.

$$\left(\frac{1}{\omega_c}\right)^2 = 6R^2 \implies \omega = \sqrt{6}R^2$$

Another example is the Colpitts Oscillator. It consists of an opamp with negative feedback, so it needs also three poles. In this case they are made by two capacitances and one coil.



Colpitts Oscillator

The feedback β loop

can be visualized as

It is not easy to

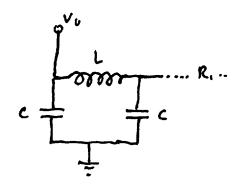
calculate $\beta = \frac{V_n}{V_0}$, but

we can make a

Simplification:

At X the teedback must

be real (imaginary part = 0). Plus, if we assume R, to be large, it must mean that the impedance from the output of the amplifier looking into the



CLC bridge must be real: $Z = \frac{1}{j\omega c} \frac{1}{i\omega L} + \frac{1}{j\omega c}$ $= \frac{1}{j\omega c} \left(\frac{j\omega L}{j\omega L} + \frac{1}{j\omega c} \right)$ $= \frac{1}{j\omega c} \left(\frac{j\omega L}{j\omega L} + \frac{1}{j\omega c} \right)$

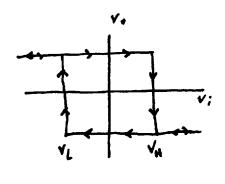
$$Z = \frac{(L/c - 1/\omega^{2}c^{2})}{j(-\frac{1}{\omega}c + \omega L - \frac{1}{\omega}c)}$$

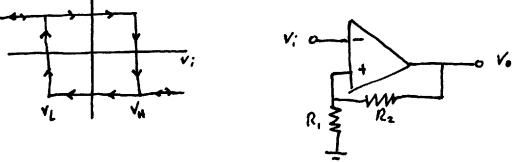
$$= \frac{-2}{\omega c} + \omega L = 0$$

$$\Rightarrow \omega = \sqrt{\frac{2}{Lc}}, \quad f = \frac{\omega}{2\pi} = \sqrt{\frac{1}{2\pi^{2}Lc}}$$

A memory element can be made of a

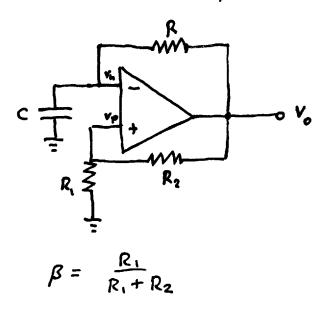
Schmitt trigger

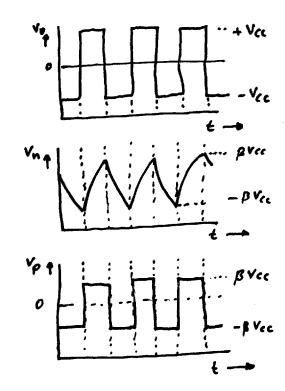




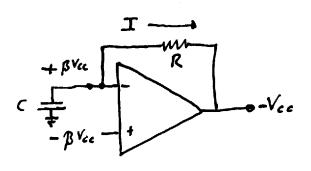
For vi=0, there are two possible states at the output + Vcc and - Vcc , depending on the history. Thus, for Vi = 0, we can read the memory element. To program the element, a voltage higher than $V_{H} = \frac{R_{i}}{R_{i} + R_{r}} V_{ce}$ should be set at V_{i} . This makes the output to - Vec (logical "O"). To program a logical "t", a voltage below $V_L = -\frac{R_1}{R_1 + R_2}$ vce should be set at the input.

A memory element is a bistable element. It can take either of two output values and is stable. Contrasting this is a Astable Multivibrator which is astable at both possible output values ± Vcc





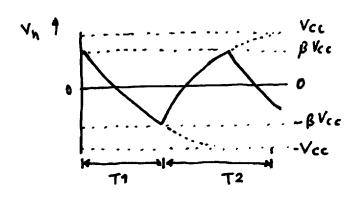
Imagine V_0 at $-V_{cc}$. V_P is then at $-\frac{R_1}{R_1+R_2}$. V_{cc} $= -\beta V_{cc}$. Imagine V_n starts at + βV_{cc} .



Through the resistance R will initially (t=0) go a current $I = (\beta V_{ce} - (-V_{ce}))/R$

This current will uncharge C! Because of this, Vn is lowering [Note that thus I is constantly reduced and is not constant) It is thus

exponentially decaying from + B Vcc to -Vcc, with an RC time of R*C. However, when it reaches - B Vcc it becomes lower than Vp. In this case the output commutes -Vcc -+ + Vcc and a reverse cycle starts.



How long does it take to charge the capacitor?

1) Starts at +
$$\beta V_{cc}$$
 ? $V_n = -V_{cc} + (\beta+1) V_{cc} \exp(-\frac{1}{4})$
2) Aluming at $-V_{cc}$ }

3) The relaxation time is
$$V_n = -V_{cc} + (\beta+1)V_{cc} \exp(-\frac{t}{Rc})$$

 $T = Rc$

4) stops at Vn = - BVcc

$$\Rightarrow T_1 = RC \ln \left(\frac{1+\beta}{1-\beta} \right)$$

In a similar way we can show that T2 = T1 and in total

$$T = 2 RC \ln \left(\frac{1+\beta}{1-\beta} \right)$$

$$f_{osc} = \frac{1}{2\pi T}$$

CHAPTER S

OUT PUT STAGES

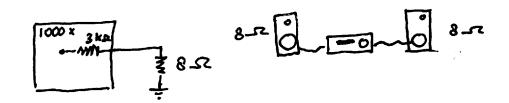
ch 9 Sedra ch 16 Bogart

up to now we have analyzed the circuits without worrying about what was connected to it. In fact, we have always assumed the ideal case, with nothing connected.

Moreover, the signals at the various stages of the amplification were alway small signals, thus guaranteeing that it was working in the linear In this way, the only trequency appearing was the one supplied at the input. at the output signal is not small, non-linearithe output This can be put in the so called ties might occur. (THD), which describes - harmonic distortion the percentage of power appearing at the 2+ fo, 3+ fo ..., etc of the fundamental

40.

Another important parameter is the output resistance fout of the total circuit. Our signal amplifiers discussed in the previous chapters (differential pair and common emitter amplifier) all had high output resistance (NRC, NKS2's). When connecting a load to this high-ohmic amplifiers, the gain will drop significantly. Consider the following amplifier to which we connect speakers (N8S2)



The gain drops from 1000 to $1000 * \frac{8}{8+3000} = 2.7$ (a factor 376!).

We need an output stage with low resistance at the output. From lectures in circuit analysis, we know that, given an amplifier with R output resistance, the maximum power transfer is when the load resistance is R.

Although the reasoning cannot be inversed (!).

we will use the expected load resistance as an indication of the desired output resistance.

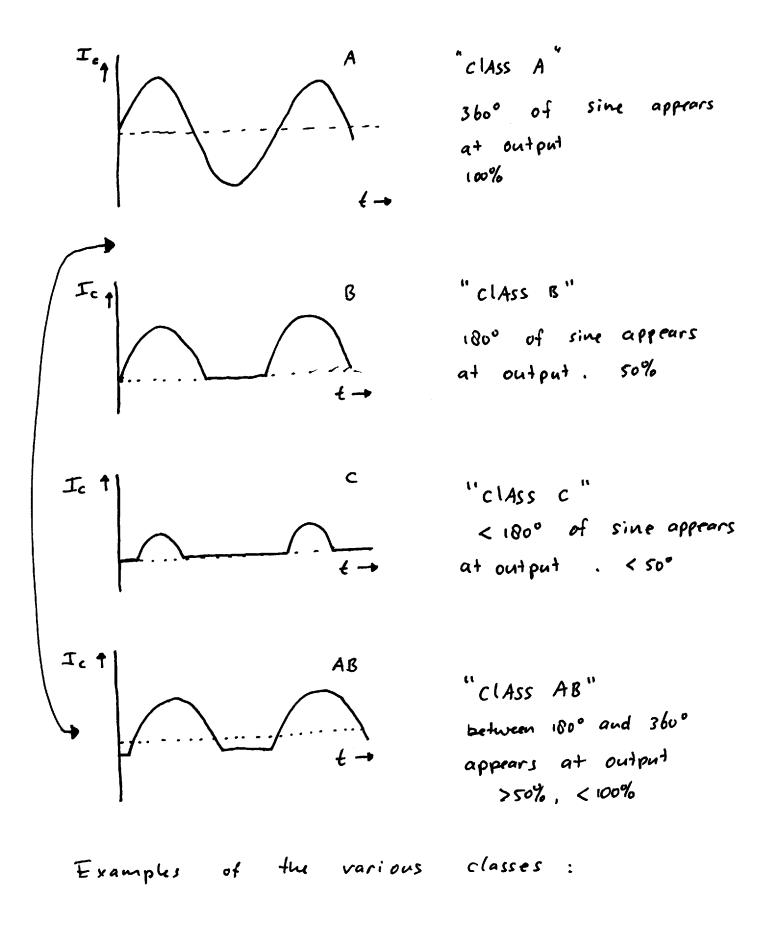
Another important aspect is the heat generated inside the components. Ideally, the heat is only generated outside the amplifier, in the load. However, significant heat can be generated in the transistors. Such transistors can overheat.

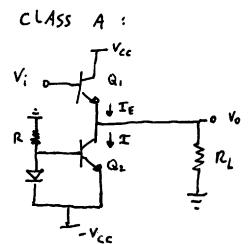
Finally, it is important to know what the output signals can be. Are they limited by any voltage (for example: only possive voltages). We will start with this.

Classification of output stages

The classification of amplifiers is based on the waveform of the collector current at the output when a sinusoidal input signal is applied.

In this way can be distinguished the various "classes" of amplifiers, see the figures on the next page.

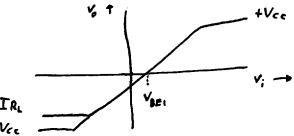




The bottom part is a

To vo Current Source defining the

RL current I. (see p. 13 of ch.1)



The gain is 1. The output voltage is limited by the power supply, either cutting at +Vec by Q1 or -Vec by Q2. Moreover, IE has to be positive. Thus Vo has to be bigger than - I.RL.

power conversion efficiency

 $\eta = \frac{P_L}{P_S}$ power at load

power supplied to output Stage

The maximum swing at vo is from - Vcc to + Vcc
The average power PL is thus

$$P_{L} = \int_{0}^{T} V(t) \cdot I(t) \cdot dt = \int_{0}^{T} V_{ce} \sin(\omega t) \cdot \frac{V_{ce}}{R_{L}} \sin(\omega t)$$

$$(T is full period) = \frac{1}{2} \frac{V_{ce}^{2}}{R_{L}}$$

The -Vcc power supply supplies a constant current of 2I (Q, + diode). The current supplied by +Vcc

swings from 0 to 2I. The average is thus I.

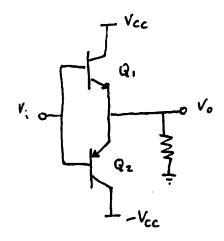
$$P_{s} = \frac{1}{\tau} \int_{0}^{\tau} (-V_{ce}) \left(-2I\right) dt + \frac{1}{\tau} \int_{0}^{\tau} \left(V_{ce} \cdot I + V_{ce} \cdot I \cdot \sin \omega t\right) dt$$

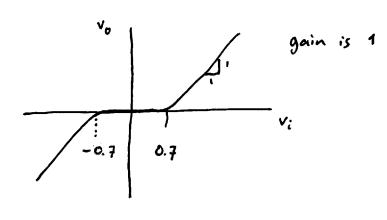
$$\eta = \frac{P_L}{P_S} = \frac{\frac{1}{2} \frac{V_{cc}^2}{R_L}}{3 V_{cc} I} = \frac{1}{6} \frac{V_{cc}}{IR_L}$$

For a good polarization $I = \frac{V_{cc}}{RL}$. Thus, the maximum efficiency is 16%.

CLASS B:

CLASS A = 2 x CLASS B





This class B output stage consists of an upn and a pup transistor in series. They cannot both conduct at the same time, thus eliminating the quiescent power consumption. The price paid is an inactive region -0.7 V... +0.7 V.

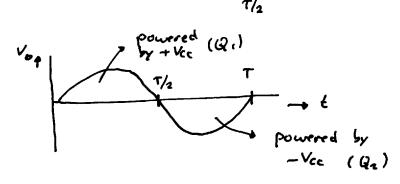
$$\eta = \frac{P_L}{P_S}$$

$$P_L$$
 is the same as the other circuit

wax

 $P_L = \frac{1}{2} V_{cc}^2 / R_L = \frac{1}{7} V_o(t) \cdot V_o(t) / R_L dt$

$$P_{s} = \frac{T/2}{T} \int_{0}^{T/2} V_{cc} \cdot \frac{V_{o}(4)}{R_{L}} dt + \frac{1}{T} \int_{0}^{T/2} -V_{cc} \cdot \frac{V_{o}(4)}{R_{L}} dt$$



max : Vo (t) = Vcc sin (wt)

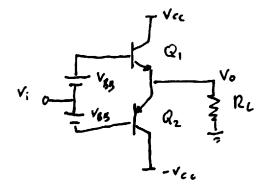
$$P_{S} = 2 \int_{0}^{T/2} \left(V_{cc}^{2} / R_{L} \right) \sin(\omega t) dt$$

$$= 4 V_{cc}^{2} / R_{L}$$

$$\eta = \frac{P_{1}}{P_{1}} = \frac{\frac{1}{h} V_{cc}^{e} / R_{L}}{\frac{4}{2\pi} V_{cc}^{e} / R_{L}} = \frac{\pi}{4} = 79 \%$$

a significant increase compared to the class A output stage of p.6

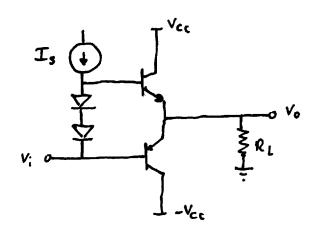
To avoid the cross-over distortion from -0.7 v to +0.7 v, the transistors can be biased. Instead of 2×B, the result is 2×AB:



 V_{gg} should be chosen in this way to marginally open the two transistors at $V_i = 0$. Too much bios

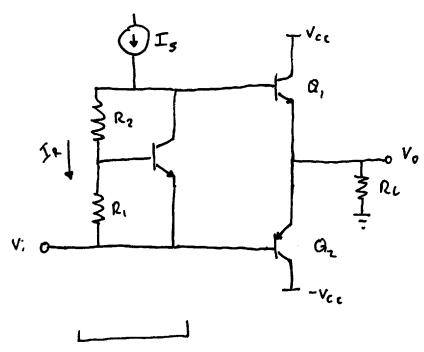
will cause an unnecessary quiescent current $(I_{E4} \neq 0 , I_{E2} \neq 0 \text{ for } V_{i} = 0). Too little bias will cause "cross-over" or "dead band",$

An elegant way to implement this is with a current source and diodes:



The diods guarantee
that both transistors
are marginally open at $v_i = 0$. (Note that v_0 $v_1 = 0.7$ $v_2 = 0.0$)

Another way to do it is by an V_{BE} multiplier (see next page)



VBE multiplier

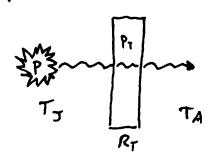
Ignoring the base current of the VBE multiplier, it can be shown that the current I_R causing a voltage drop of V_{BE} (0.7 V) in R_1 must cause a voltage drop of $R_2 \cdot I_R = R_2 \cdot \frac{V_{BE}}{R_1}$ in resistance R_2 . The total drop in the V_{BE} multiplier is thus

$$V_{BE} + \frac{R_2}{R_1} V_{BE} = V_{BE} \left(1 + \frac{R_2}{R_1} \right)$$

Heat generated by transistors

A Transistor cannot exceed a temperature of 150°C - 200°C. With higher temperatures they get distroyed irreversibly

The power generated inside a transistor causes a rise in temperature of the junction. This heat is transported to the ambient



transistor ambient

TA: ambient temperature

Tj: junction temperature

P: Power generated at

junction

PT: Power transported to

ambient

RT: Thermal resistance of

package.

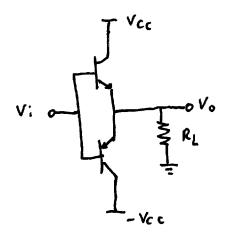
The transport of heat to the ambient, P_T, is limited by the thermal conductivity of the materials (package, air, etc.). This can be modelled by the parameter R_T, the thermal resistivity. The heat transported is proportional to the temp. gradient:

$$P_{\tau} = (T_5 - T_A)/R_{\tau}$$

when equilibrium is established, the heat transported is equal to the heat generated, P. It is easy to show that the final temperature is then

(Note: unit of RT is K/W or C/W)

Example



$$R_L = 8 - 22$$
, $R_T = 80 \text{ k/w}$, $T_A = 25^{\circ}\text{C}$
we want 25 W output power
 $P_L = 25 \text{ W}$

Since
$$P_L = \frac{1}{2} V_{cc}^2 / R_L$$
, we design $V_{cc} = 20 V$

Then

$$P_{L} = \frac{1}{2} V_{cc}^{2} / R_{L} = \frac{1}{2} 20^{2} / 8 = 25 W$$

$$P_{S} = \frac{2}{11} V_{cc}^{2} / R_{L} = 31.8 W$$

power dissipated inside the transistors

$$P = P_s - P_L = 6.8 W$$

Per transistor

Then, the junction temperature will be

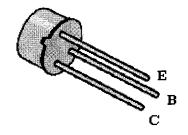
T₃ = 25°C + 3.4 W * 80°C/W = 297°C

This transistor will burn! A way to prevent this is to use special metal transistors where the collector (which generates most of the heat) is in direct contact with the metal case and use heat

Sinks. or use ventilators on top of the transistors

Simple transistor
with plastic packing
ex. BC 549

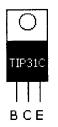
2N2222



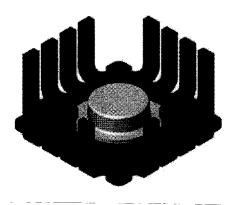
transistor with metal casing ex. 2n2222

FRONT VIEW

Decreasing



TIP31C TRANSISTOR transistor with heat sink to screw to circuit board



transistor with metal case and extended heat sink Below is a schematic of a 741" operational amplifier. Identify the input stage (differential pair of ch.1) and output stage of this chapter. (copied from Sedra, p. 812)

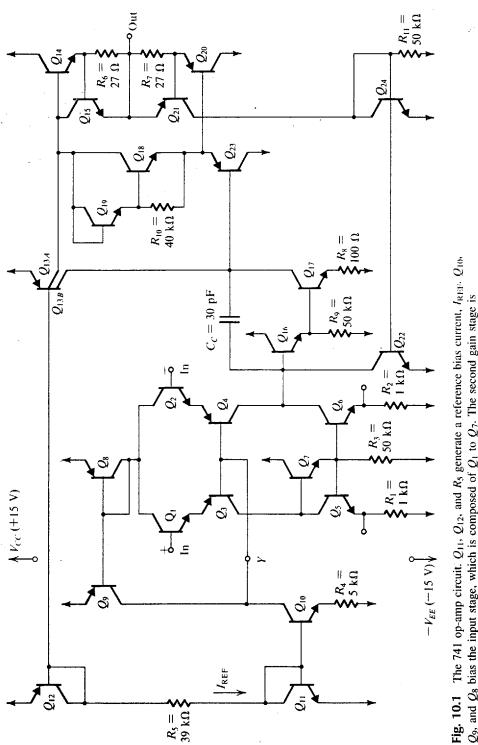


Fig. 10.1 The 741 op-amp circuit. Q_{11} , Q_{12} , and R_8 generate a reference bias current, I_{REE} : Q_{10} , Q_9 , and Q_8 bias the input stage, which is composed of Q_1 to Q_7 . The second gain stage is composed of Q_{16} and Q_{13} with Q_{138} acting as active load. The class AB output stage is formed by Q_{14} and Q_{20} with biasing devices Q_{134} , Q_{18} and Q_{19} , and an input buffer Q_{23} . Transistors Q_{15} , Q_{24} , and Q_{22} serve to protect the amplifier against output short circuits and are normally off.