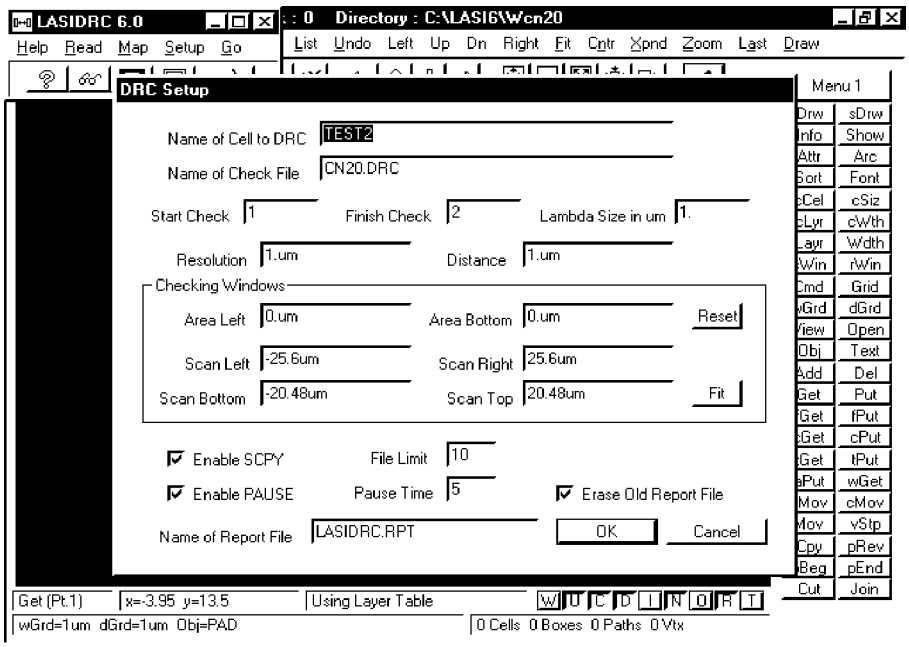
2.2.2 Using the LasiDrc Program

To perform a design rule check (DRC) of a layout, simply select **LasiDrc**, from the LASI system menu, followed by **Setup**. Enter the name of the cell (see below) to be checked and type cn20.drc as the name of the check file. Since we only know two design rules at this point, that is, from Fig. 2.7 checks 1 and 2, the starting check should be 1 and the finish check should be 2. To start the program, select **Go** on the top of the LASIDRC screen (after closing the setup screen). If there is an error a bit map of the layout will be generated (and can be viewed with the **Map** command) and the error will be reported in a report file (which can be read using the **Read** command). The DRC will be performed on the *section* of layout shown in the drawing display just prior to calling the LASIDRC program or after the **Save** command is used if the DRC program is already open. To DRC the entire cell, press the **Fit** command button on the DRC setup screen. This feature can be used to decrease the time it takes to perform a DRC by DRCing only the specific areas of interest.



2.3 Resistance Calculation

In addition to serving as a region in which to build PMOS transistors, n-wells are sometimes used to create integrated resistors. The resistance of a material is a function of the materials resistivity, ρ, and the materials dimensions. For example, the slab of material in Fig. 2.8 between the two leads has a resistance given by