# CHAPTER 5

## OUTPUT STAGES

ch 9 Sedra
ch 16 Bogart

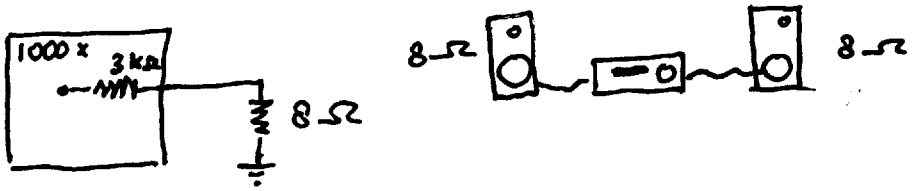
---

Up to now we have analyzed the circuits without worrying about what was connected to it. In fact, we have always assumed the ideal case, with nothing connected.

Moreover, the signals at the various stages of the amplification were alway small signals, thus guaranteeing that it was working in the linear regime. In this way, the only frequency appearing at the output was the one supplied at the input.

when the output signal is not small, non-linearities might occur. This can be put in the so called total-harmonic distortion (THD), which describes the percentage of power appearing at the harmonics $2*f_0$, $3*f_0$ ..., etc of the fundamental $f_0$.

Another important parameter is the output resistance $r_{out}$ of the total circuit. Our signal amplifiers discussed in the previous chapters (differential pair and common emitter amplifier) all had high output resistance ($\sim R_c$, $\sim$ k$\Omega$'s). When connecting a load to this high-ohmic amplifiers, the gain will drop significantly. Consider the following amplifier to which we connect speakers ($\sim 8\,\Omega$)




The gain drops from 1000 to $1000 \cdot \frac{8}{8+3000} = 2.7$ (a factor 376 !).

We need an output stage with low resistance at the output. From lectures in circuit analysis, we know that, given an amplifier with $R$ output resistance, the maximum power transfer is when the load resistanee is $R$.

Although the reasoning cannot be inversed (!),

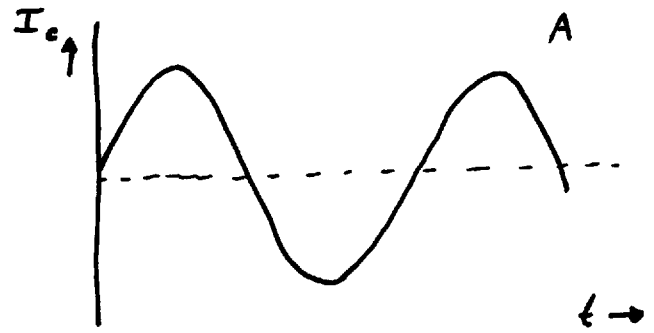
we will use the expected load resistance as an indication of the desired output resistance.

Another important aspect is the heat generated inside the components. Ideally, the heat is only generated outside the amplifier, in the load. However, significant heat can be generated in the transistors. Such transistors can overheat.

Finally, it is important to know what the output signals can be. Are they limited by any voltage (for example: only possive voltages). We will start with this.

## Classification of output stages

The classification of amplifiers is based on the waveform of the collector current at the output when a sinusoidal input signal is applied.
In this way can be distinguished the various "classes" of amplifiers, see the figures on the next page.




"class A"

360° of sine appears at output 100%


"class B"

180° of sine appears at output. 50%


"class C"

< 180° of sine appears at output . < 50°

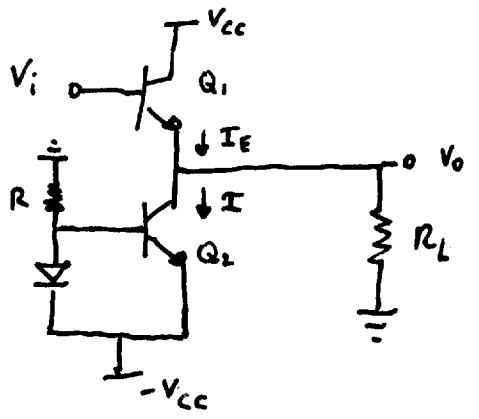

"class AB"

between 180° and 360° appears at output

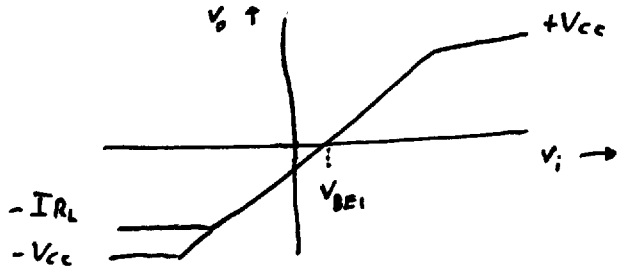
>50%, <100%

Examples of the various classes :

CLASS A :




The bottom part is a current source defining the current $I$. (see p. 13 of ch. 1)




The gain is 1. The output voltage is limited by the powe supply, either cutting at $+V_{cc}$ by $Q_1$ or $-V_{cc}$ by $Q_2$. Moreover, $I_E$ has to be positive. Thus $V_o$ has to be bigger than $-I \cdot R_L$.

power conversion efficiency

$$\eta \equiv \frac{P_L}{P_s}$$

$P_L$ ← power at load

$P_s$ ← power supplied to output stage

The maximum swing at $V_o$ is from $-V_{cc}$ to $+V_{cc}$

The average power $P_L$ is thus

$$P_L = \int_0^T V(t) \cdot I(t) \cdot dt = \int_0^T V_{cc} \sin(\omega t) \cdot \frac{V_{cc}}{R_L} \sin(\omega t)$$

(T is full period)

$$= \frac{1}{2} \frac{V_{cc}^2}{R_L}$$

The $-V_{cc}$ power supply supplies a constant current of $2I$ ($Q_2$ + diode). The current supplied by $+V_{cc}$

swings from 0 to $2I$. The average is thus $I$.

$$P_s = \frac{1}{T}\int_0^T (-V_{cc})\cdot(-2I)\,dt + \frac{1}{T}\int_0^T (V_{cc}\cdot I + V_{cc} I \sin \omega t)\,dt$$

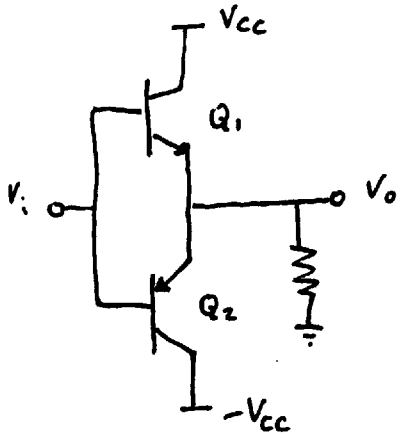
$$= 3 V_{cc} I$$

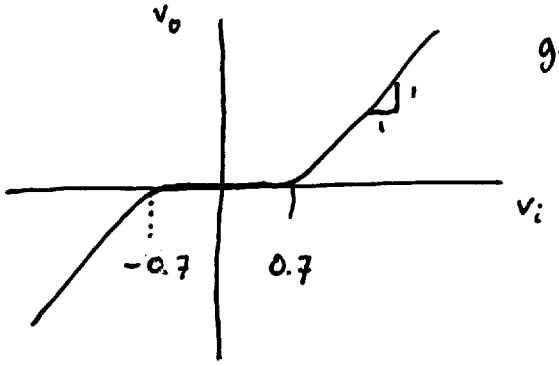
$$\eta = \frac{P_L}{P_s} = \frac{1/2\ V_{cc}^2/R_L}{3 V_{cc} I} = \frac{1}{6}\frac{V_{cc}}{I R_L}$$

For a good polarization $I = V_{cc}/R_L$. Thus, the maximum efficiency is 16%.

---

CLASS B: CLASS A = 2 × CLASS B




gain is 1

This class B output stage consists of an npn and a pnp transistor in series. They cannot both conduct at the same time, thus eliminating the quiescent power consumption. The price paid is an inactive region $-0.7\ V \ldots +0.7\ V$.

maximum efficiency : (ignoring the $2 \times 0.7$ V losses)

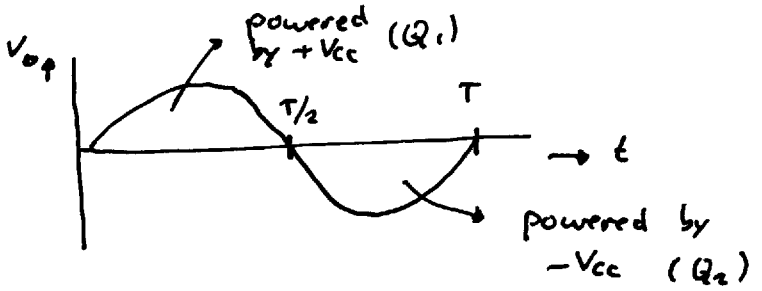
$$\eta = \frac{P_L}{P_S}$$

$P_L$ is the same as the other circuit

$$P_L^{max} = 1/2\ V_{cc}^2 / R_L = \frac{1}{T}\int_0^T V_o(t) \cdot V_o(t)/R_L\ dt$$

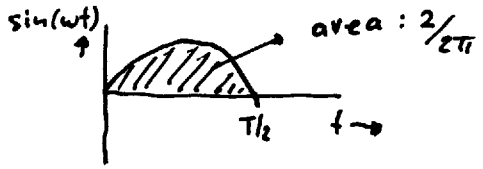
$P_S$ is different. $P_S = \frac{1}{T}\int_0^T V_{cc} \cdot I_{cc}\ dt$

$$P_S^{max} = \frac{1}{T}\int_0^{T/2} V_{cc} \cdot \frac{V_o(t)}{R_L}\ dt + \frac{1}{T}\int_{T/2}^{T} -V_{cc} \cdot \frac{V_o(t)}{R_L}\ dt$$




max : $V_o(t) = V_{cc} \sin(\omega t)$

$$P_S = \frac{2}{T}\int_0^{T/2} (V_{cc}^2/R_L) \sin(\omega t)\ dt$$

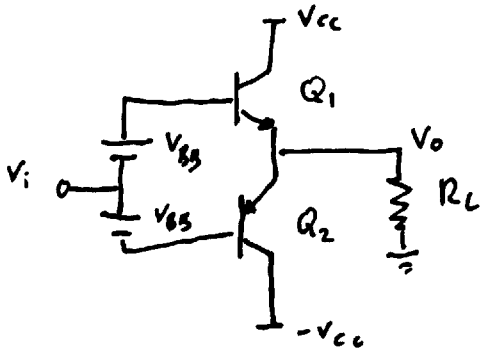



$$= \frac{4}{2\pi} V_{cc}^2 / R_L$$

$$\eta = \frac{P_L}{P_S} = \frac{1/2\ V_{cc}^2/R_L}{4/2\pi\ V_{cc}^2/R_L} = \frac{\pi}{4} = 79\ \%$$

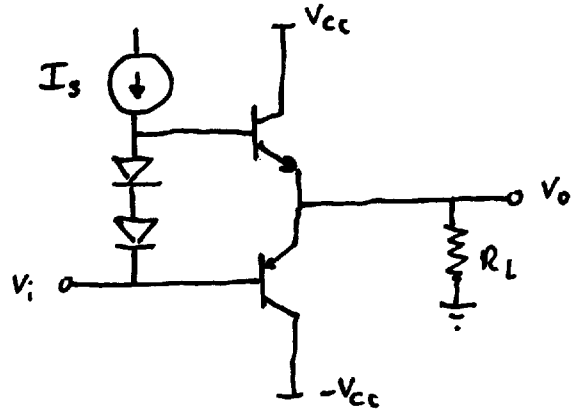
a significant increase compared to the class A output stage of p. 6

To avoid the cross-over distortion from $-0.7$ V to $+0.7$ V, the transistors can be biased. Instead of 2 x B, the result is 2 x AB:




$V_{BB}$ should be chosen in this way to marginally open the two transistors at $V_i = 0$. Too much bias will cause an unnecessary quiescent current ($I_{E1} \neq 0$, $I_{E2} \neq 0$ for $V_i = 0$). Too little bias will cause "cross-over" or "dead band".

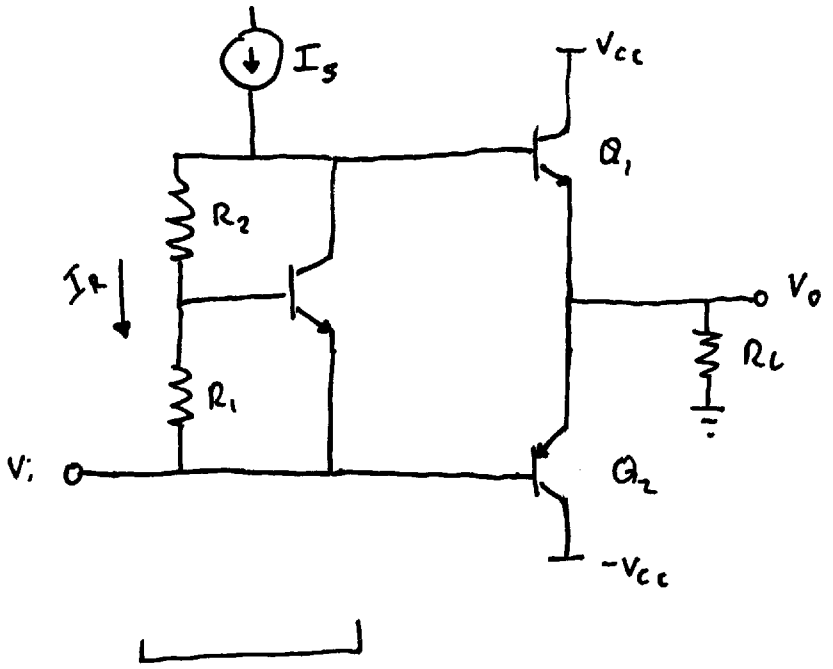
An elegant way to implement this is with a current source and diodes:




The diodes guarantee that both transistors are marginally open at $V_i = 0$. (Note that $V_o = 0.7$ V for $V_i = 0$ V)

Another way to do it is by an $V_{BE}$ multiplier

(see next page)




$V_{BE}$ multiplier

Ignoring the base current of the $V_{BE}$ multiplier, it can be shown that the current $I_R$ causing a voltage drop of $V_{BE}$ (0.7 V) in $R_1$ must cause a voltage drop of $R_2 \cdot I_R = R_2 \cdot \frac{V_{BE}}{R_1}$ in resistance $R_2$. The total drop in the $V_{BE}$ multiplier is thus

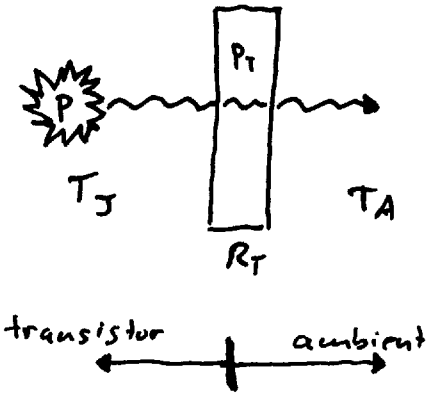
$$V_{BE} + \frac{R_2}{R_1} V_{BE} = V_{BE} \left(1 + R_2/R_1\right)$$

---

## Heat generated by transistors

A Transistor cannot exceed a temperature of 150°C – 200°C. With higher temperatures they get distroyed irreversibly

The power generated inside a transistor causes a rise in temperature of the junction. This heat is transported to the ambient




$T_A$ : ambient temperature
$T_J$ : junction temperature
P : Power generated at junction
$P_T$ : Power transported to ambient
$R_T$ : Thermal resistance of package.

The transport of heat to the ambient, $P_T$, is limited by the thermal conductivity of the materials (package, air, etc.). This can be modelled by the parameter $R_T$, the thermal resistivity. The heat transported is proportional to the temp. gradient:

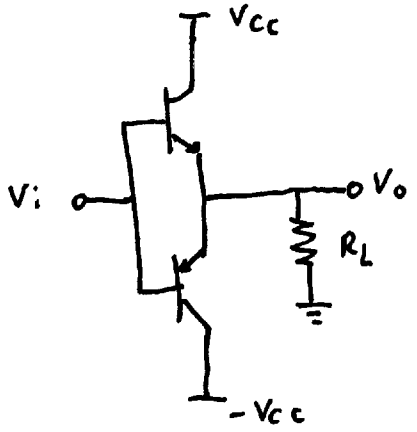
$$P_T = (T_J - T_A)/R_T$$

When equilibrium is established, the heat transported is equal to the heat generated, P. It is easy to show that the final temperature is then

$$T_J = T_A + P \cdot R_T$$

(Note: unit of $R_T$ is K/W or °C/W)

Example




$R_L = 8\ \Omega$ , $R_T = 80\ k/W$, $T_A = 25\ ^\circ C$

we want 25 W output power

$P_L^{max} = 25\ W$

Since $P_L^{max} = 1/2\ V_{cc}^2 / R_L$ , we

design $V_{cc} = 20\ V$

Then

$$P_L = \frac{1}{2} V_{cc}^2 / R_L = \frac{1}{2}\ 20^2 / 8 = 25\ W$$

$$P_S = \frac{2}{\pi} V_{cc}^2 / R_L = 31.8\ W$$

power dissipated inside the transistors

$$P = P_S - P_L = 6.8\ W$$

Per transistor

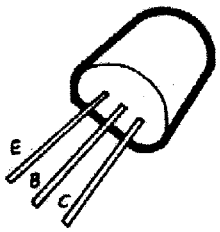
$$P = 3.4\ W$$

Then, the junction temperature will be

$$T_J = 25\ ^\circ C + 3.4\ W \times 80\ ^\circ C/W = 297\ ^\circ C$$

This transistor will burn! A way to prevent this is to use special metal transistors where the collector (which generates most of the heat) is in direct contact with the metal case and use heat sinks. or use ventilators on top of the transistors

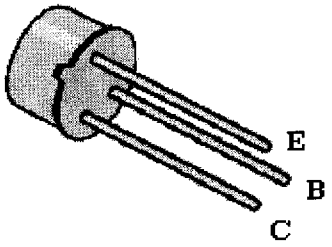
Decreasing $R_T$




BC 549

← Simple transistor with plastic packing
ex. BC 549

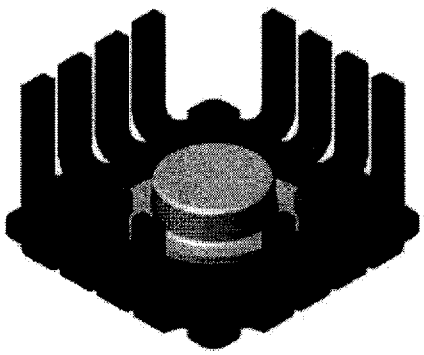
2N2222




← transistor with metal casing
ex. 2N2222


TIP31C
TRANSISTOR

← transistor with heat sink to screw to circuit board



← transistor with metal case and extended heat sink

Below is a schematic of a "741" operational amplifier. Identify the input stage (differential pair of ch. 1) and output stage of this chapter. (copied from Sedra, p. 812)

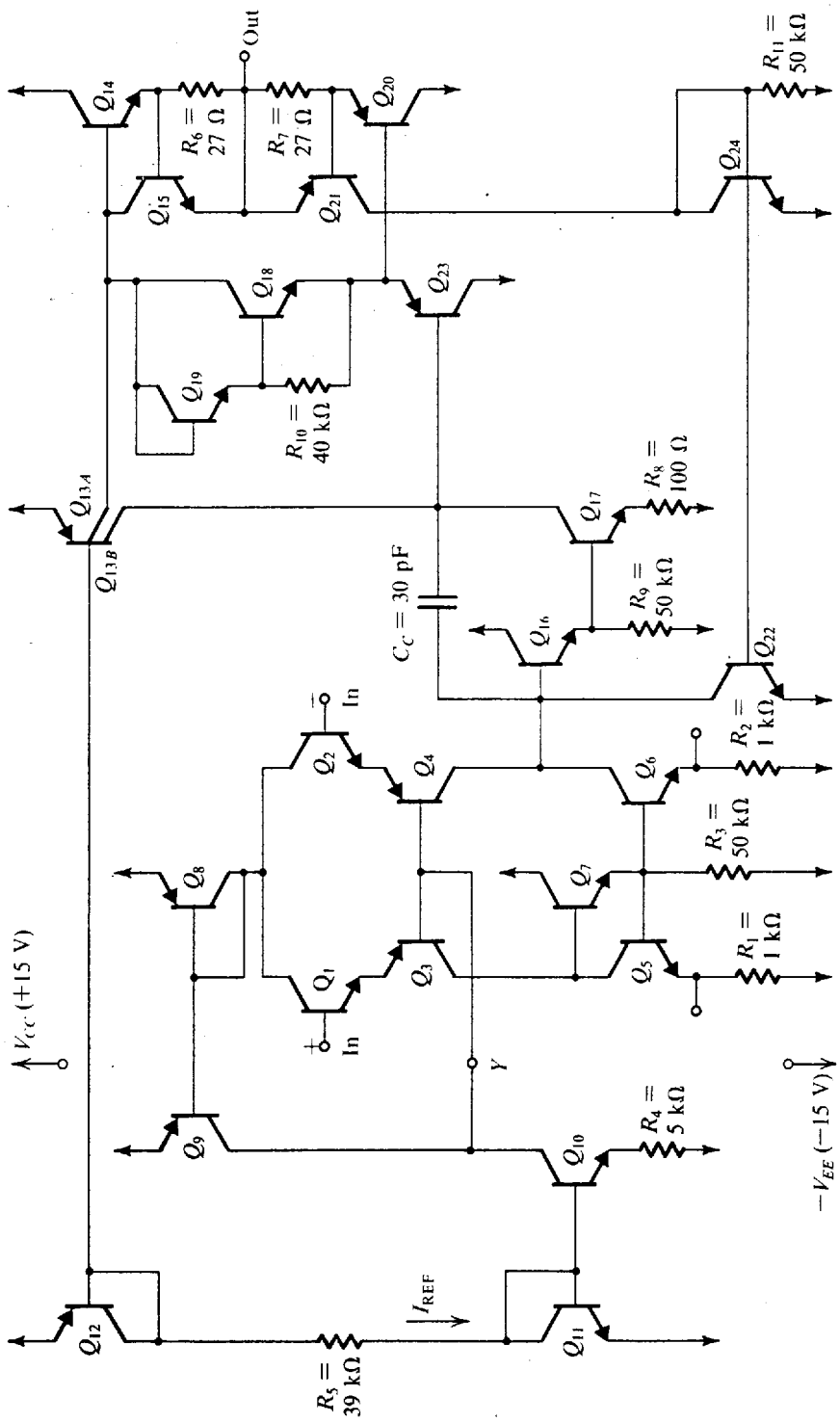



**Fig. 10.1** The 741 op-amp circuit. $Q_{11}$, $Q_{12}$, and $R_5$ generate a reference bias current, $I_{REF}$. $Q_{10}$, $Q_9$, and $Q_8$ bias the input stage, which is composed of $Q_1$ to $Q_7$. The second gain stage is composed of $Q_{16}$ and $Q_{17}$ with $Q_{13B}$ acting as active load. The class AB output stage is formed by $Q_{14}$ and $Q_{20}$ with biasing devices $Q_{13A}$, $Q_{18}$ and $Q_{19}$, and an input buffer $Q_{23}$. Transistors $Q_{15}$, $Q_{21}$, $Q_{24}$, and $Q_{22}$ serve to protect the amplifier against output short circuits and are normally off.