Lab 4: Operational Amplifier

Introduction

The operational amplifier (opamp) is a device that performs amplification of its two input voltages. Opamps are often used as means of detecting and amplifying error in feedback systems. Non-inverting and inverting amplifiers based on an opamp are good examples of applications of an opamp in feedback systems.

In this lab, you are to analyze, simulate, and test the basic CMOS opamp shown in Figure 1. The supply voltage (V_{DD}) is 5 V in this lab.

Preparation

Go through the following preparation steps for the opamp in Figure 1.

1. Find parametric expressions for differential gain (A_d), common-mode gain (A_c), common-mode rejection ratio (CMRR), and the bandwidth $f_{3\text{dB}}$ assuming a load capacitance of C_L.

2. Find the numerical values for A_d, A_c, CMRR, and $f_{3\text{dB}}$ for $I_B = 1$ mA and $C_L = 1$ nF.

3. Find the input common-mode voltage that maximize the output swing.

4. Decompose the opamp input in Figure 2 input into differential and common-mode components by hand analysis. In other words, express the differential and common-mode components of the opamp input in Figure 2 in terms of v_s.

5. Show that the differential gain of an opamp can be found using a single signal source as shown in Figure 2 as long as $A_d \gg A_c$. This is the setup you will use in the lab since a differential signal generator is not available in the lab. *Hint:* $A_d \equiv v_o/(v_{ip} - v_{in})$ *and* $A_c \equiv 2v_o/(v_{ip} + v_{in})$.

6. Run AC simulations to show A_d, A_c and CMRR at low frequencies. Also run a DC simulation to show the output swing with a differential input with the common-mode voltage found in 3. Label and comment on the plots to clearly show the results.

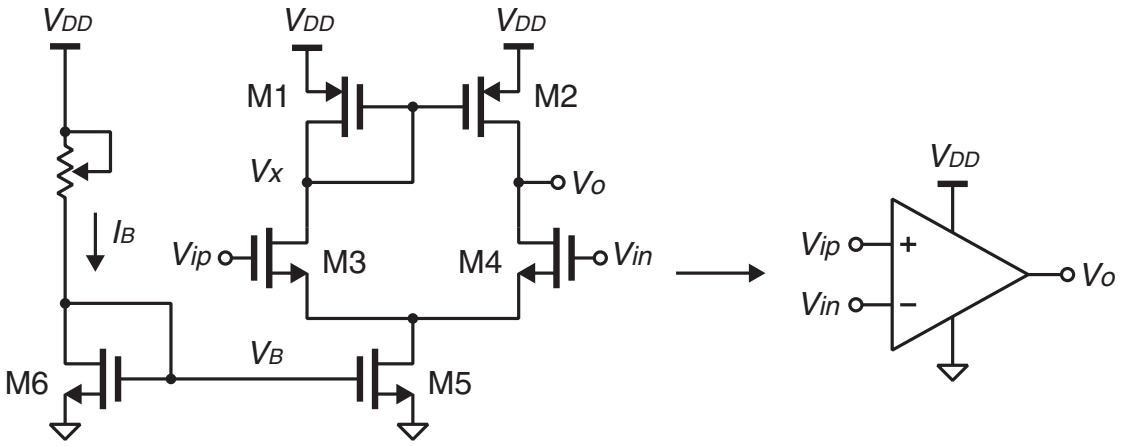

Figure 1: A CMOS opamp.

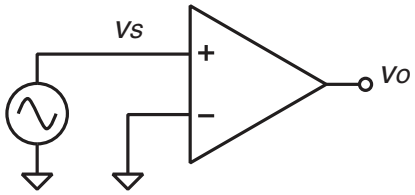

Figure 2: An opamp with a single-ended input.

Table 1: Minimum parts list

Part	Description	Quantity
ALD1101	NMOS transistor pair	2
ALD1102	PMOS transistor pair	1
-	10-kΩ multi-turn potentiometer	3

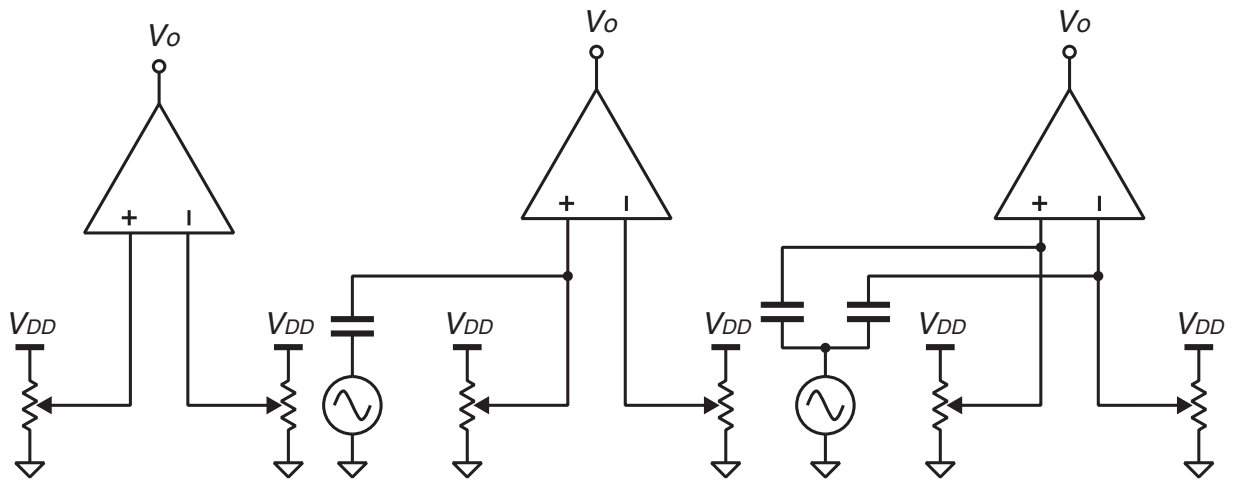

Figure 3: (a) Circuit configurations for offset cancellation, (b) differential gain (A_d) measurement, and (c) common-mode gain (A_c) measurement.

Lab

A minimum parts list for this lab is shown in Table 1. This is the absolute minimum. You may bring more parts for your convenience and backup.

1. Assemble the opamp shown in Figure 1 on the breadboard
2. Adjust the bias current (I_B) to 1 mA, and set the opamp inputs to the common-mode voltage found in preparation using two multi-turn potentiometers asshown in Figure 3(a) .
3. Adjust one of the opamp input for $V_o = V_x$ (see Figure 1) where the opamp is at equilibrium. The opamp differential input at the equilibrium is the offset voltage of the opamp. Do not turn the potentiometers from this point.
4. Connect one of the opamp inputs to a signal generator via a large capacitor as shown in Figure 3(b) and find the differential gain (A_d) of the opamp.
5. Connect both of the opamp inputs to a signal generator via separate capacitors as shown in Figure 3(c) and find the common-mode gain (A_c) of the opamp. Calculate the CMRR.
6. Insert a 1-nF load capacitor at the opamp output and find the $f_{3\text{dB}}$.
7. Compare the experimental results with simulation. Explain and justify any discrepancy.

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Preparation

1. $A_d = -g_{m4}(r_{o4}||r_{o2})$
   $A_c = -g_{m4}r_{o4}\frac{1/g_{m2}}{2g_{me4}r_{o4}r_{o5}+1/g_{m2}} \approx -1/2g_{m2}r_{o5}$
   CMRR $= A_d/A_c = 2g_{m2}g_{m4}r_{o5}(r_{o4}||r_{o2})$
   $f_{3\text{dB}} = 1/2\pi(r_{o4}||r_{o2})C_L$

2. $A_d = -65.1 = 36.3$ dB
   $A_c = -1/231.8 = -47.3$ dB
   CMRR $= 83.6$ dB
   $f_{3dB} = 5.18$ kHz

3. $V_{CM} = V_{ov5} + V_{gs4} = 667$ mV $+ 1.18$ V $= 1.85$ V

4. $v_d = v_{ip} - v_{in} = v_s - 0 = v_s$
   $v_c = (v_{ip} + v_{in})/2 = (v_s + 0)/2 = v_s/2$

5. $v_o = A_d v_d + A_c v_c = A_d v_s + A_c v_s/2 = v_s(A_d + A_c/2) \approx A_d v_s$
   Then, $A_d \approx v_o/v_s$.

6. See Figures 1 and 2.
   $A_d = 33.6$ dB
   $A_c = -44.4$ dB
   CMRR $= 78.0$ dB

Lab

- The measured common-mode gain should be much more than calculated/simulated due to the transistor mismatch.
- The averaging feature of the oscilloscope may be needed to show the small input voltage required to prevent clipping of the output. Proper triggering is essential for correct measurements. Use a reliable clean signal (either the opamp output or sync out of the signal source) as a trigger source.

APPENDIX

ALD1101 (NMOS) and ALD 1102 (PMOS) model

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* ALD ALD1101 (NMOS) and ALD 1102 (NMOS) model
* This model was extracted from measurements.
* The model is correct only for W = 1738 um and L = 1 um.
* The device size above doesn't represent the actual device
size.

* NMOS hand analysis values: Vtn = 0.71 V; UnCox(W/L) = 4.5
mA/V^2 ; VA = 80 V;

* PMOS hand analysis values: Vtn = -0.65 V; UpCox(W/L) =
2.10 mA/V^2 ; VA = -19 V;
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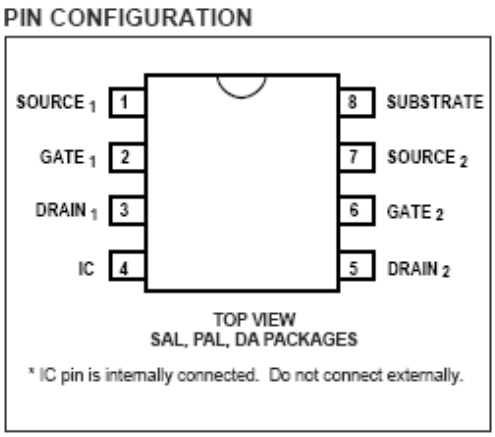
PIN CONFIGURATION

ALD1101 (NMOS)



ALD 1102 (PMOS)