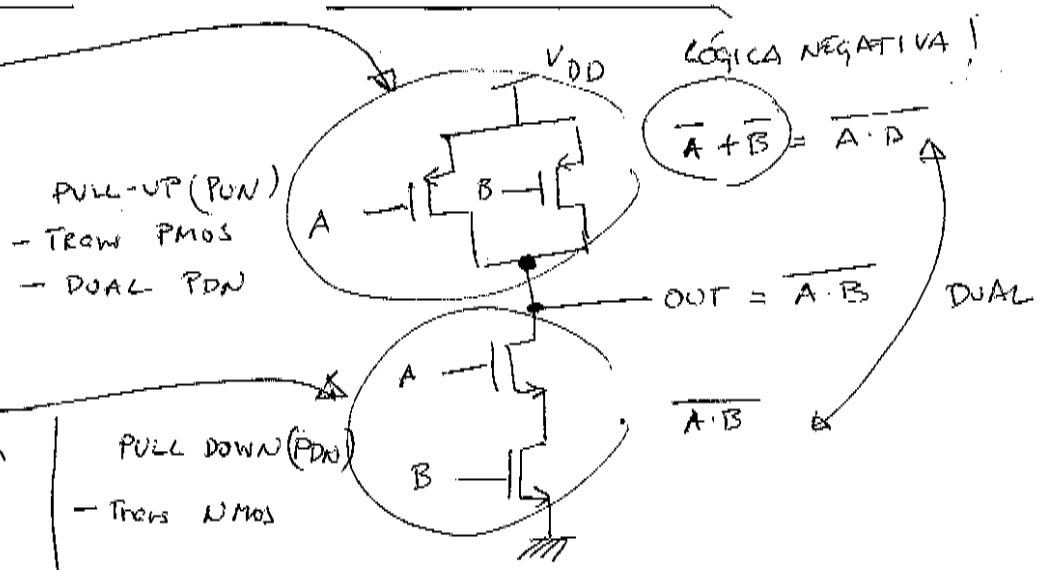
MICROELECTRÓNICA AULA 6

PORTAS NAND E NOR. LÓGICA COMBINATÓRIA

NAND

A	B	A·B	$\overline{A \cdot B}$
0	0	0	1
0	1	0	1
1	0	0	1
1	1	1	0



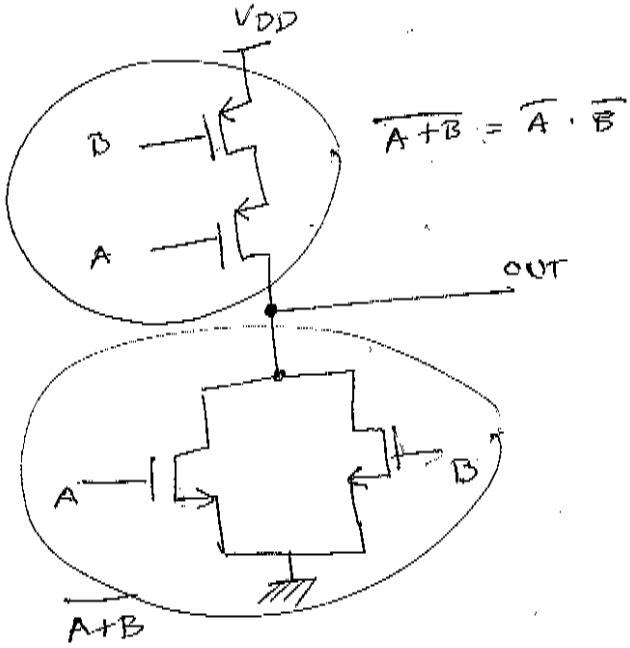
Leis de De Morgan

$\overline{A+B} = \overline{A} \cdot \overline{B}$

$\overline{A \cdot B} = \overline{A} + \overline{B}$

NOR

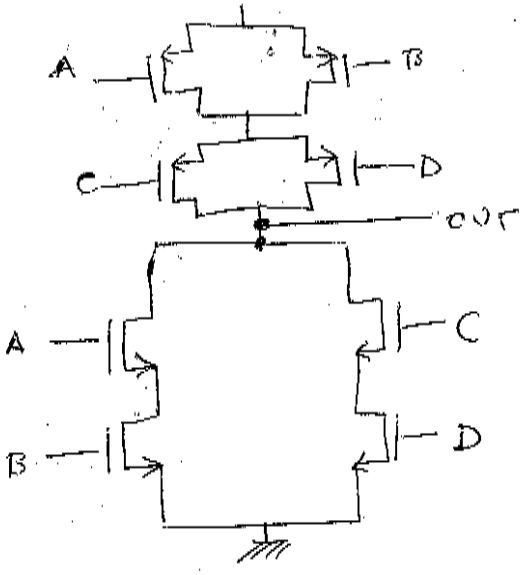
A	B	A+B	$\overline{A+B}$
0	0	0	1
0	1	1	0
1	0	1	0
1	1	1	0



CIRCUITOS COMPLEXOS EM LÓGICA COMPLEMENTAR

Exemplo Implementar $F = \overline{[(A \cdot B) + (C \cdot D)]} = \overline{A \cdot B} \cdot \overline{C \cdot D}$

$= (\overline{A} + \overline{B}) \cdot (\overline{C} + \overline{D})$



Exemplo Implementar $Z = \overline{A} + BC$

$$Z = \overline{\overline{A} + BC}$$

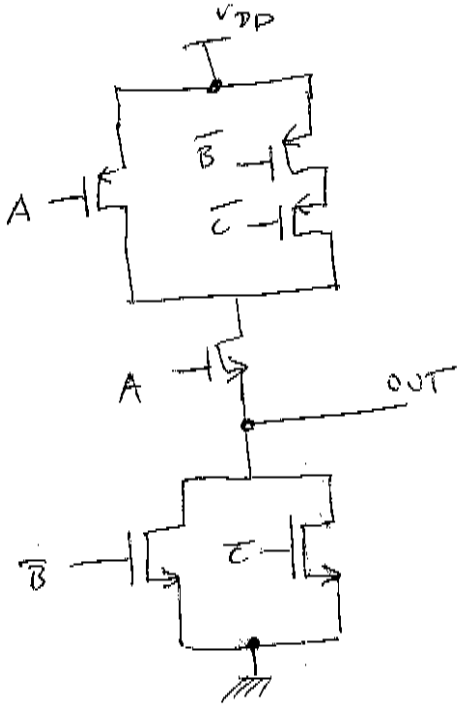
$$Z = \overline{\overline{A} \cdot \overline{BC}}$$

$$Z = \overline{A \cdot (\overline{B} + \overline{C})} \leftarrow PDN$$

$$Z = \overline{A \cdot (\overline{B} + \overline{C})}$$

$$= \overline{A} + \overline{(\overline{B} + \overline{C})}$$

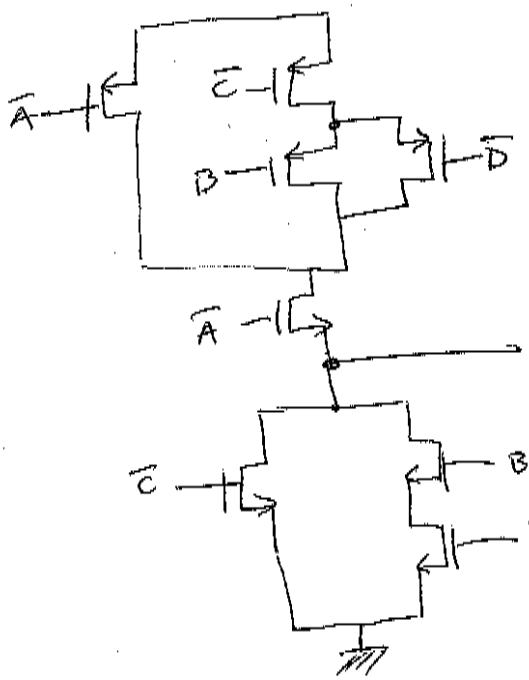
$$= \overline{A} + (\overline{\overline{B}} \cdot \overline{\overline{C}}) \leftarrow PUN$$



Exemplo Implementar $Z = A + \overline{B}C + CD = A + C \cdot (\overline{B} + D)$

$$Z = \overline{\overline{A + C \cdot (\overline{B} + D)}} = \overline{\overline{A} \cdot \overline{C \cdot (\overline{B} + D)}}$$

$$= \overline{\overline{A} \cdot [\overline{C} + (\overline{B} + D)]} = \overline{\overline{A} \cdot [\overline{C} + (B \cdot \overline{D})]}$$



$$Z = \overline{\overline{A} \cdot [\overline{C} + B\overline{D}]}$$

$$= \overline{\overline{A}} + \overline{(\overline{C} + B\overline{D})}$$

$$= \overline{\overline{A}} + (\overline{\overline{C}} \cdot \overline{B\overline{D}}) = \overline{\overline{A}} + (\overline{\overline{C}} \cdot (\overline{B} + \overline{\overline{D}}))$$

Exemplo Implementar a porta OU exclusivo XOR

A	B	XOR
0	0	0
0	1	1
1	0	1
1	1	0

$$XOR = \overline{\overline{A}B} + A\overline{B} = \overline{\overline{\overline{A}B}} \cdot \overline{A\overline{B}}$$

$$= \overline{(A+\overline{B}) \cdot (\overline{A}+B)}$$

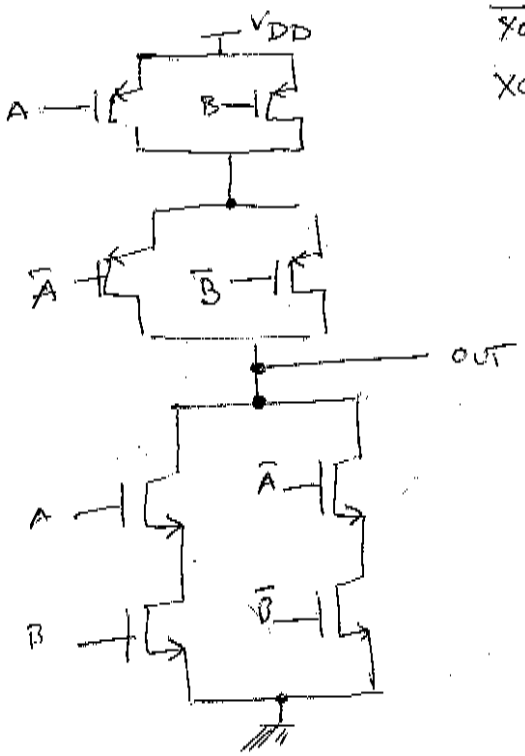
ALTERNATIVA

$$\overline{XOR} = \overline{A}\overline{B} + AB$$

$$XOR = \overline{\overline{A}\overline{B} + AB}$$

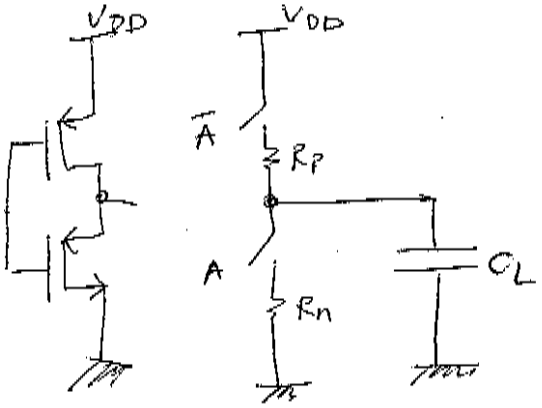
$$= \overline{\overline{A}\overline{B}} \cdot \overline{AB}$$

$$= \left(\overline{\overline{A}} + \overline{\overline{B}}\right) \cdot (\overline{A} + \overline{B})$$



DIMENSIONAMENTO DOS TRANSISTORES PARA $t_{PLH} = t_{PHL}$

Exemplo INVERSOR



$$I_D = KP \frac{W}{L}\left((V_{GS} - V_T) V_{DS} - \frac{V_{DS}^2}{2}\right)$$

$$I_D \simeq KP \frac{W}{L}(V_{GS} - V_T) V_{DS}$$

$$\frac{1}{R} = \frac{\partial I_D}{\partial V_{DS}} = KP \frac{W}{L}(V_{GS} - V_T) \Big|_{V_{DD}}$$

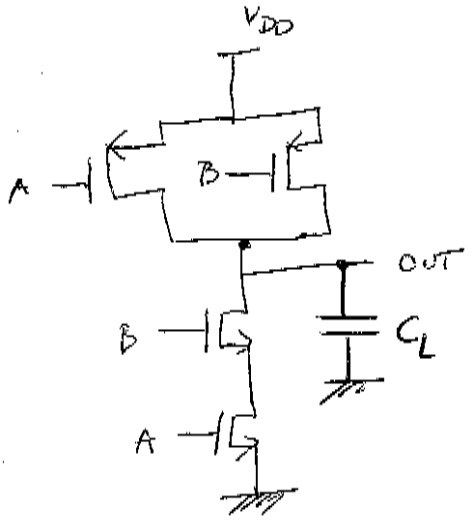
$$\frac{V_{DD}}{2} = V_{DD}\, e^{-t/RC}$$

$$t_{PLH} \simeq 0.69\, R_P C_L$$

$$t_{PHL} \simeq 0.69\, R_N C_L$$

IDEAL $t_{PLH} = t_{PHL} \iff R_P = R_N$

NAND



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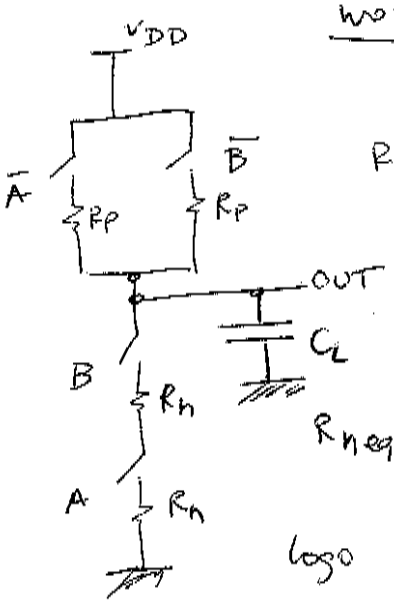
WORST CASE



$R_{p\,equivalente} = R_p$

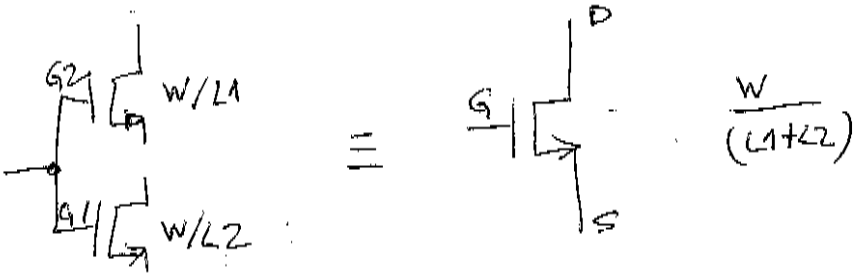
$R_{n\,equivalente} = 2 \times R_n$

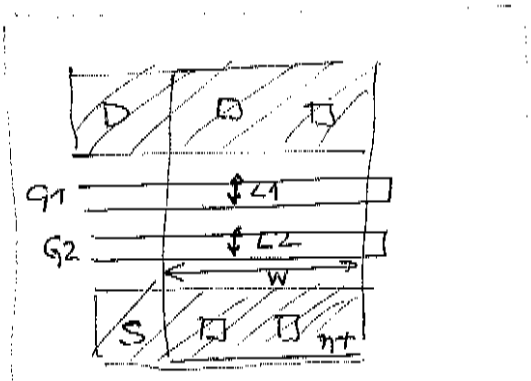
logo $t_{pHL} = 2\, t_{pLH}$

a menos que se diminua o valor de R_n para metade (factor $1/2$)

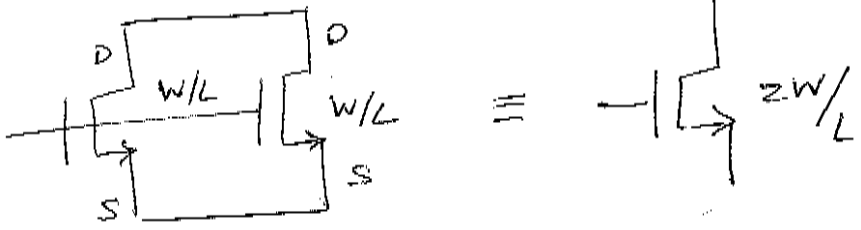
Recapitulando

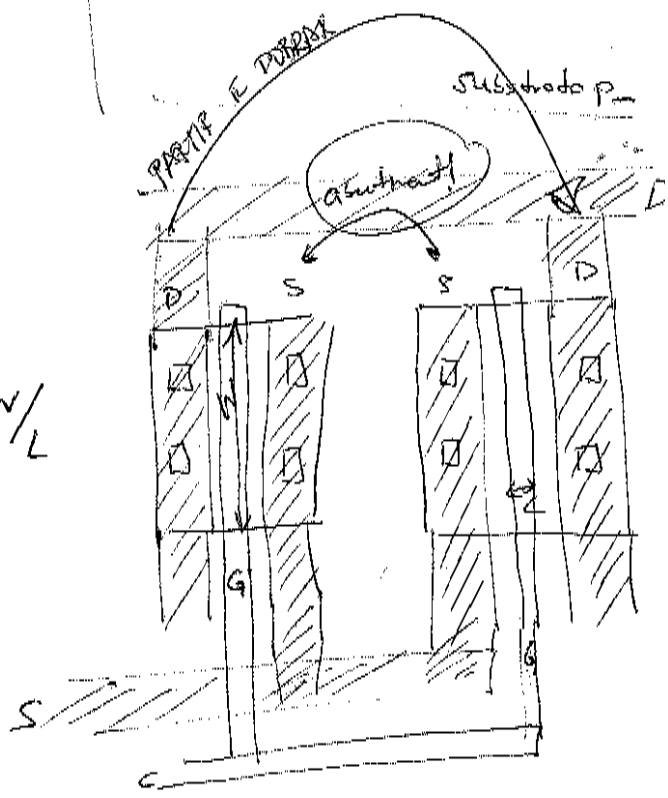
transistores em série





transistores em paralelo

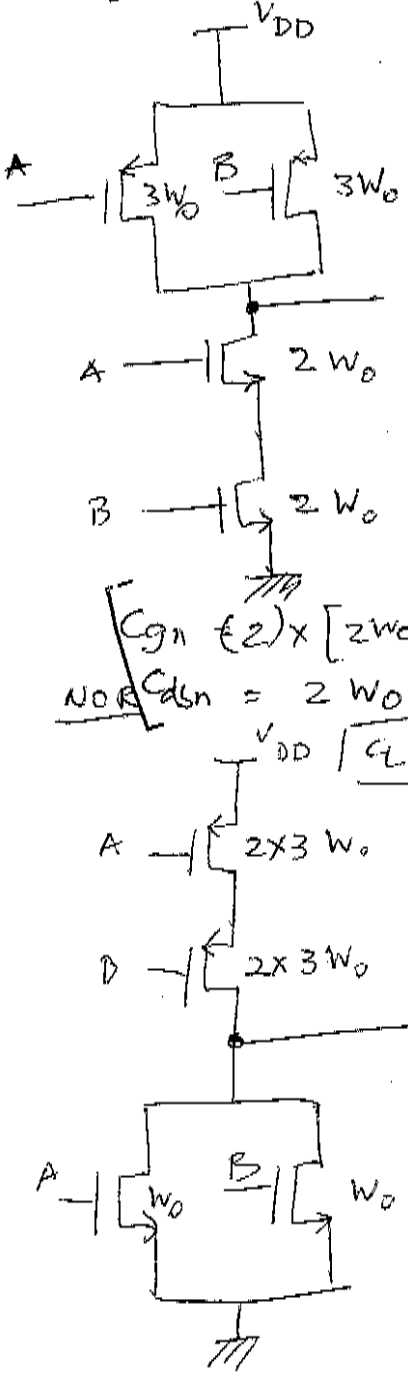




SOLUÇÃO

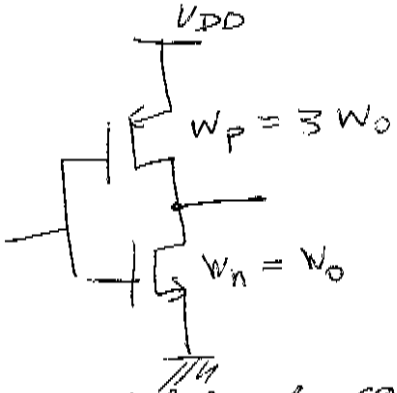
Sendo $\mu_n = 3\mu_p \Rightarrow W_p = 3 W_n$

NAND



$t_p = 2 t_{p0}$

INVERSOR



$t_p = t_{p0}$

Capacidade de carga intrínseca

$C_L = (C_{gn} + C_{gp}) + (C_{dbn} + C_{dbp})$

$[C_{gn} \text{ (2)} \times [2W_0 \times L] C_{ox}$

NOR $C_{dbn} = 2 W_0$ Lde CDB $]$

$C_L = (2+\alpha) C_{gn} + (2+\alpha) C_{dbn} = (1+\alpha) C_{gn} + (1+\alpha) C_{dbn}$

$t_p = 0.69 R_n C_L$

$t_p \propto C_L$

$C_{gn} = W_0 L C_{ox}$

$C_{db} = W_0$ Lde CDB

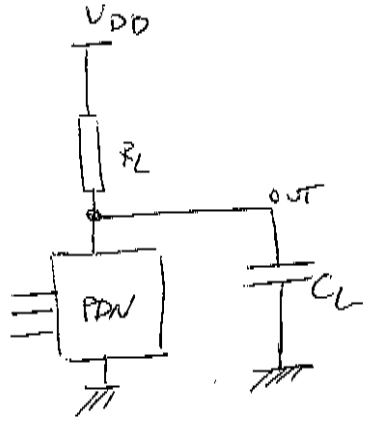
$C_L = (1+2\alpha) C_{gn} + (1+2\alpha) C_{dbn}$

NAND $t_p \cong N \; t_{p0}$ Sendo N o número de entradas

NOR Muito embora o NOR seja mais lento que o NAND

OUTRAS FAMILIAS LÓGICAS

RATIOED LOGIC — Lógica baseada numa divisão de tensão

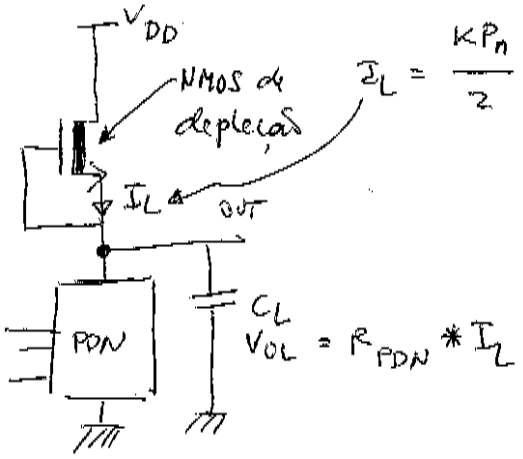


$$V_{OL} = \frac{R_{PDN}}{R_L + R_{PDN}} V_{DD}$$

ideal $R_L >> R_{PDN}$

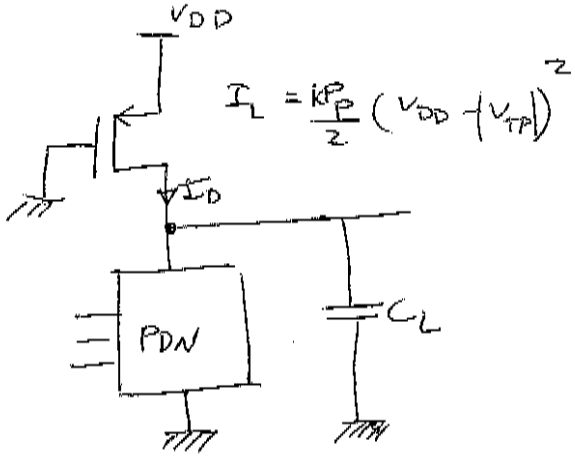
MAS R_L grande significa $t_{pLH} >> t_{pHL}$

NMOS LOGIC



$$I_L = \frac{kP_n}{2} |V_{Tn}|^2$$

PSEUDO-NMOS



$$I_L = \frac{kP_p}{2}(V_{DD} - |V_{TP}|)^2$$

V_{OL} calculado com PMOS EM SATURAÇÃO NMOS EM ZONA LINEAR

$$I_D = \left(\frac{W}{L}\right)_n kP_n \left[(V_{DD} - V_{Tn}) V_{OL} - \frac{V_{OL}^2}{2}\right] = \frac{1}{2}\left(\frac{W}{L}\right)_p kP_p (V_{DD} - |V_{TP}|)^2$$

para $V_{TP} = V_{Tn}$, $V_{OL} = (V_{DD} - V_T)\left(1 - \sqrt{1 - \frac{kP_p}{kP_n}}\right)$

ideal $\left(\frac{W}{L}\right)_n kP_n >> kP_p \left(\frac{W}{L}\right)_p$

$V_M \longrightarrow (V_{IN} = V_{OUT})$

PMOS zona linear

NMOS em saturação

$$I_D = \frac{kP_n}{2}\left(\frac{W}{L}\right)_n (V_M - V_{Tn})^2 = \frac{kP_p}{1}\left(\frac{W}{L}\right)_p \left[(V_{DD} - |V_{TP}|)(V_{DD} - V_M) - \frac{(V_{DD} - V_M)^2}{2}\right]$$

$$V_M = V_T + (V_{DD} - V_T)\sqrt{\frac{kP_p\left(\frac{W}{L}\right)_p}{kP_n\left(\frac{W}{L}\right)_n + kP_p\left(\frac{W}{L}\right)_p}}$$

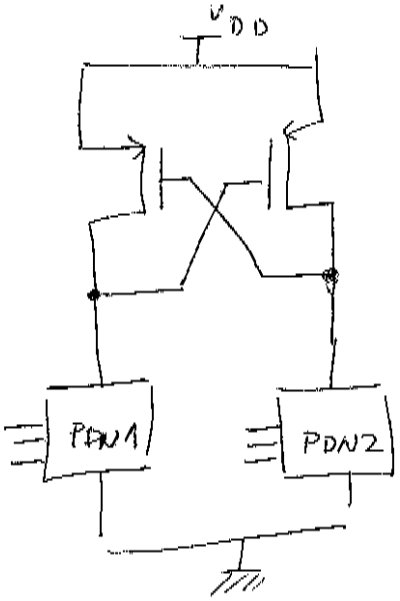
Problema — função de transferência assimétrica

— mau dimensionamento $\Longrightarrow$ porta não funciona

— dissipação estática de potência $P = V_{DD} \times \frac{kP_p}{2}\left(\frac{W}{L}\right)(V_{DD} - |V_{TP}|)^2$

DIFFERENTIAL CASCADE VOLTAGE LOGIG (DCVSL)

- Princípio dois PDNs que são complementares



OBJECTIVO Eliminar o consumo estático de corrente

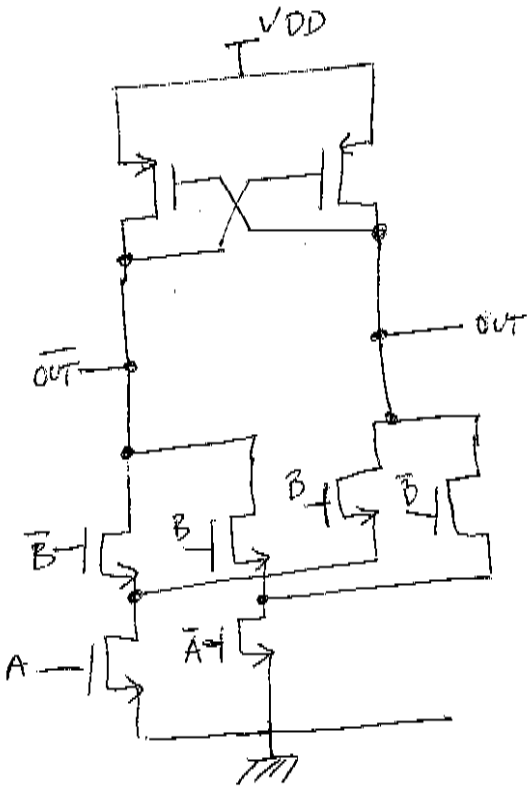
$$PDN2 = \overline{PDN1}$$

EXEMPLO OU EXCLUSIVO

A	B	XOR	$\overline{XOR}$
0	0	0	1
0	1	1	0
1	0	1	0
1	1	0	1

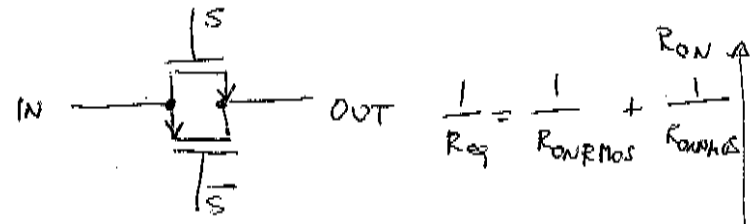
$$XOR = A\bar{B} + \bar{A}B$$

$$\overline{XOR} = \bar{A}\bar{B} + AB$$

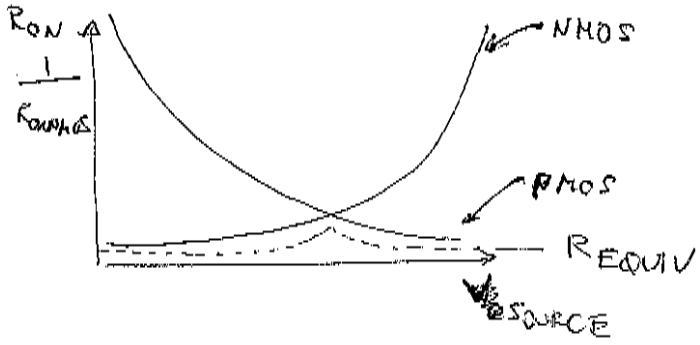


PASS TRANSISTOR LOGIC

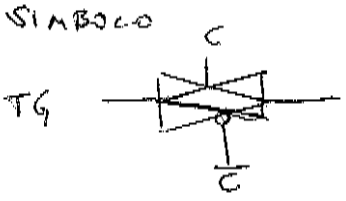
Transmission gate (porta de transmissão)



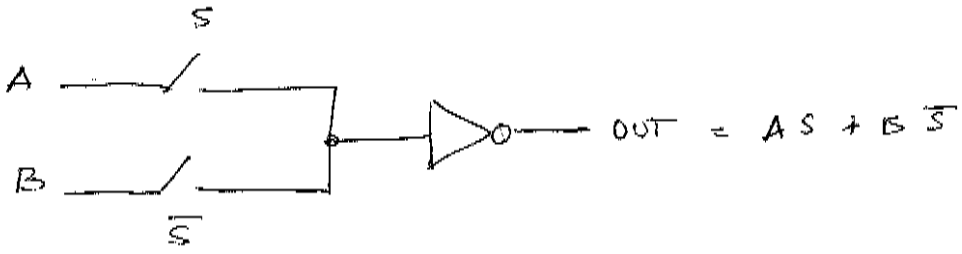
$$\frac{1}{R_{eq}} = \frac{1}{R_{ONRMOS}} + \frac{1}{R_{ONPMOS}}$$

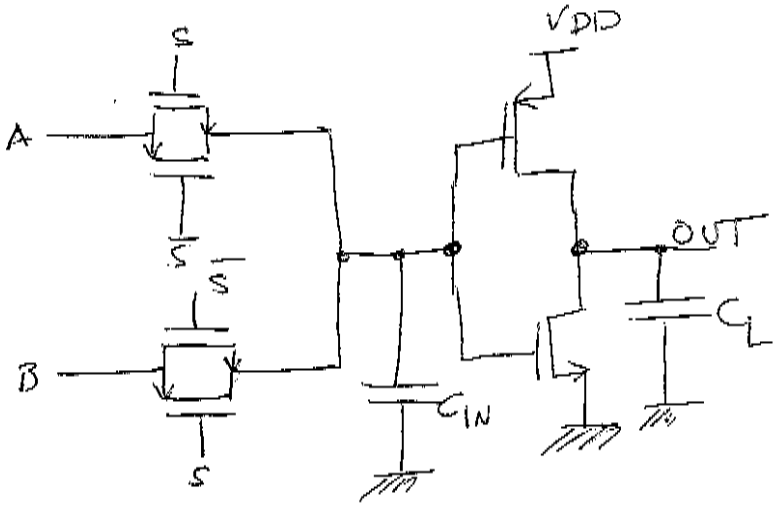


SIMBOLO



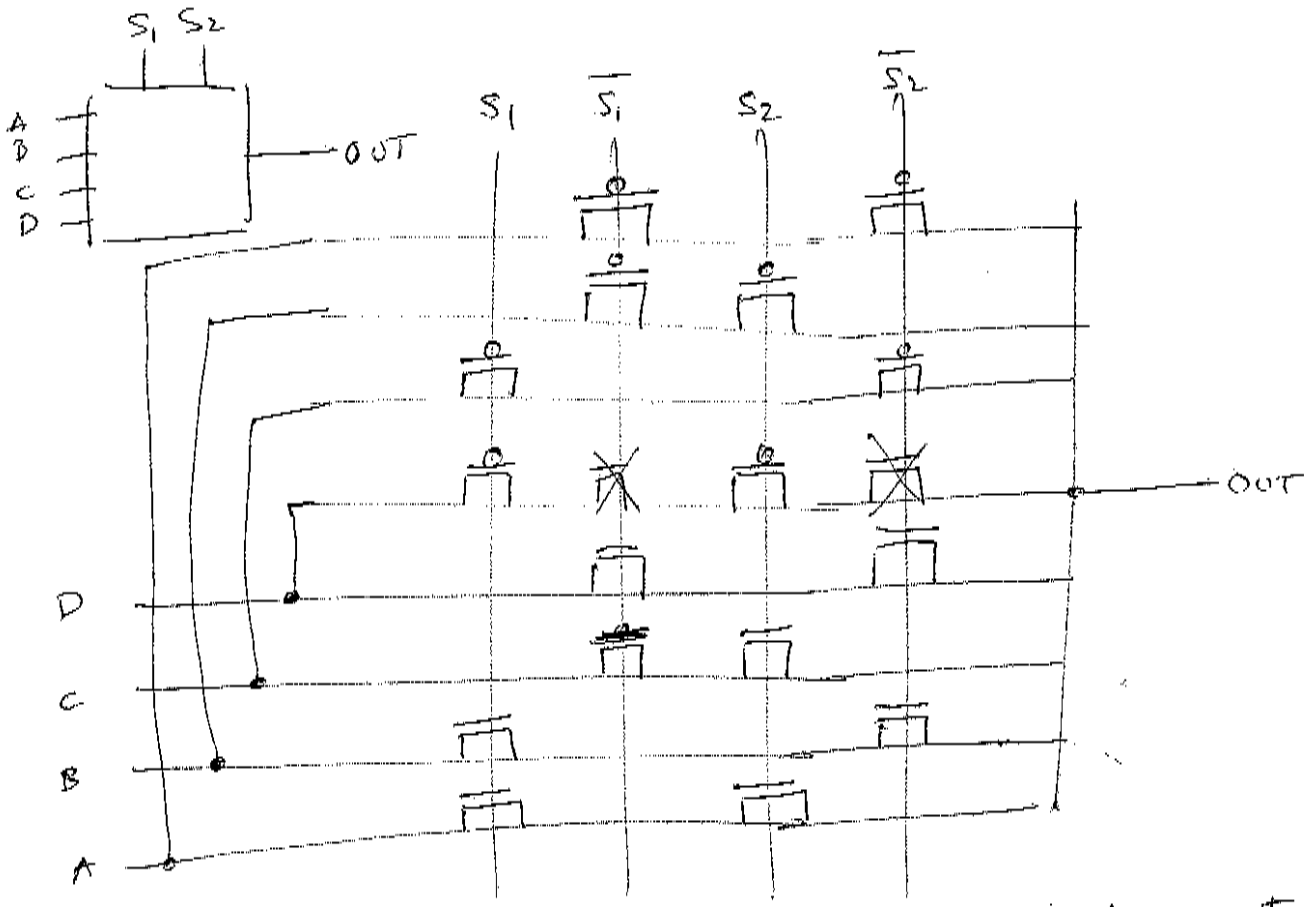
EXEMPLO: MULTIPLEXER DE 2 ENTRADAS





MULTIPLEXER DE 4 ENTRADAS

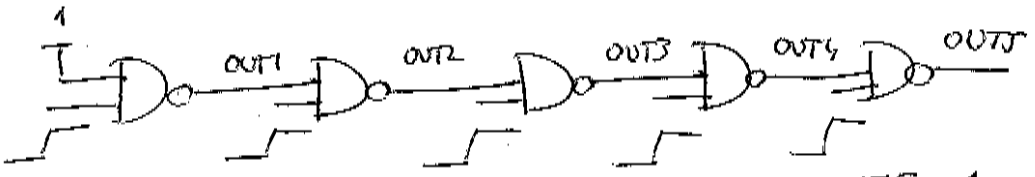
$$OUT = A(S_1 \cdot S_2) + B(S_1 \cdot \overline{S_2}) + C(\overline{S_1} \cdot S_2) + D(\overline{S_1} \cdot \overline{S_2})$$



O multiplexer é tb o de-multiplexer — basta inverter o sentido dos sinais! NOTAR ainda que isto é um MX DEMUX ANALÓGICO!

ISSUE GLITCHES — Ocorrem pois os tempos de propagação não são iguais para todos os sinais.

Exemplo



CONDIÇÃO INICIAL OUT1 = OUT2 = OUT3 = OUT4 = OUT5 = 1

Ao fim de 1 tp todas as saídas vem temporariamente a 0 !